Yeo Kiat Seng

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Professor Yeo Kiat Seng received the B.Eng. (EE) in 1993, and Ph.D. (EE) in 1996 both from Nanyang Technological University (NTU), Singapore. Currently, he is Associate Provost (Research and International Relations), Singapore University of Technology and Design (SUTD). Yeo is a widely known authority in low-power RF/mm-wave IC design and a recognized expert in CMOS technology. He was a Member of Board of Advisors of the Singapore Semiconductor Industry Association. Before his appointment at SUTD, Yeo was Associate Chair (Research), Head of Division of Circuits and Systems, Sub-Dean (Student Affairs) and Founding Director of VIRTUS of the School of Electrical and Electronic Engineering at NTU. He has published 9 books, 7 book chapters, over 600 international top-tier refereed journals and conference papers and holds 38 patents. In addition, Yeo holds/held key positions in many international conferences as Advisor, General Chair, Co-General Chair and Technical Chair. In 2009, Yeo was awarded the Public Administration Medal (Bronze) on National Day 2009 by the President of the Republic of Singapore and the Nanyang Alumni Achievement Award by NTU for his outstanding contributions to the university and society. Yeo is an IEEE Fellow for his contributions to low-power integrated circuit design.

Biography[1]

Professor Yeo Kiat Seng, IEEE Fellow

Education

Yeo graduated with a Bachelor of Engineering Honours (Electrical Engineering) in 1993 and Doctor of Philosophy (Electrical Engineering) in 1996, both from Nanyang Technological University (NTU), Singapore.

Career

Yeo began his academic career in 1993 in Nanyang Technological University (NTU), Singapore's School of Electrical and Electronic Engineering and taught circuits and systems, low-power integrated circuit design, visible light communications, CMOS technology, RF/mm-wave integrated circuit design, VLSI/ULSI design and memory. He was promoted to Professor in 2009. Yeo spent 13 years in management positions as Associate Chair (Research), Head of Circuits and Systems and Sub-Dean (Students Affairs) in NTU. He was also a Fellow of the Renaissance Engineering Programme (REP) and served as Senator and Advisory Board Member at NTU. Currently, he is Associate Provost (Research and International Relations), Singapore University of Technology and Design (SUTD). Yeo has about 30 years of experience in industry, academia and consultancy.

Yeo is a Council Member for the Singapore-Zhejiang Economic & Trade Council (SZETC), a Member of the Management Board of Temasek Laboratories at SUTD, the Republic Polytechnic's (RP) Distinguished Academic, a Distinguished Visiting Academician to Changi General Hospital (CGH), a Member of the MIT-SUTD Collaboration Governing Board, a Member of Ngee Ann Polytechnic's Expert Panel for School of Engineering, an Advisor to Hwa Chong Institution's Board of Integrated Programme, a Member of SIA Engineering Company Technology Advisory Committee, a Member of Singapore Semiconductor Industry Association Complex Equipment Consortium and an Editorial Board Member of Journal of Electronics/Circuit and Signal Processing. He has also contributed as Chairman, Co-Chair and Member of several national/society as well as industry/professional services. Yeo was a Member of Board of Advisors of the Singapore Semiconductor Industry Association, a Council Member of the Assembly & Test WSQ Framework Industry Skills and Training of the Singapore Workforce Development Agency, and Chairman of Engineering Science Advisory Committee at Ngee Ann Polytechnic.

Research

Yeo has an unquestionably prolific record of scholarships and is highly regarded as a leading authority in the field of low-power IC design (RF/mm-wave). He has a rare combination of modeling, design, fabrication and test knowledge and experience. As a result, his research has been multifaceted and highly innovative. His research achievements and contributions in IC design have been recognized in both academia and industry. Many of his publications have been shown to hold the benchmark for several low-power RF/mm-wave transceiver modules, filters and circuits. For example, his team was the first to propose the *Transformed Radial Stubs* to realize wideband low-pass filters. Based on a new filter topology, his team fabricated the world's smallest on-chip low-pass filter (US Patent 9154104) with the broadest stop-band up to 52 times the cut-off frequency, i.e., 110GHz has been achieved. The measured pass-band insertion loss is less than 2.2 dB and its size is only 350μm by 280μm.

Yeo's research combines both originality and depth to produce revolutionary results that have major practical ramifications for the electronics/semiconductor industry. He has been a technical consultant to several multinational companies such as Toshiba, Samsung, GLOBALFOUNDRIES and Sony. As a result of his excellent research track record, he has attracted research funding of more than SGD70m (~USD50m) from the industry and various funding agencies. Apart from his outstanding research, Yeo is an excellent teacher who seeks to inspire and draw out the very best in his students. He has supervised more than 120 research fellows, postdocs as well as PhD and Master's students, many of whom went on to emulate his spirit of innovation in academia and industry.

In 1997, Yeo established the first R&D facility in Asia to conduct a full range of RF/mm-wave research from characterization and modelling, design, simulation, test and measurement to verification, qualification and standardization. He subsequently founded *VIRTUS*, an IC Design Centre of Excellence, in 2009, to spearhead cutting edge IC design research for applications in medical technology, clean technology and consumer electronics. The *VIRTUS* is a SGD50m (~USD36m) mega research centre jointly funded by NTU and Singapore Economic Development Board (EDB). With his exemplary leadership in IC design, NTU was ranked 16th in the world and among the top 3 in Asia in 2008 IC Design Research Ranking for Worldwide Universities.

One of the major global mega-trends sweeping the world recently is wireless communication solutions built in computers and IT applications. As Moore's Law has passed its prime, it is getting harder to deliver performance. Energy considerations also pose stringent limits on the growth of applications, wherein portability and hence battery life are extremely important. Yeo's team is one of the most successful research groups in the world to lead pioneering research

and innovation in low-power mm-wave IC technology, and translate them into impactful solutions and commercial products. The *VIRTUS*' 60GHz transceiver System-on-Chip can support a data rate of 1Gbps over a distance of 1,000m. It is also fully compliant with IEEE 802.11ad standard and can support video streaming up to 10m. The chip incorporates time division duplexing and operates in the unlicensed 57 to 66 GHz band. Special highlights include an unconventional 36G/24G front-end transceiver architecture with carrier suppression and ultra-low unwanted emissions (US Patent 9083437), and power amplifier and linearization techniques using active and passive devices (US Patent 9130511).

Future Research Directions

The Integrated Circuit (IC) design process is one of the most complex and resource intensive processes in the design field. The time taken to design and validate the IC design can take months and the design of mixed-signal/RF/mm-wave ICs is usually a laborious process.

With the adventures in Artificial Intelligence (AI), the time has come to use AI technology to develop a common IC design knowledge database. This Intellectual Property (IP) database will be used to develop intelligent methodologies to accelerate and automate the IC design process, IC chip manufacturing process and eventually democratize IC chip design.

AI techniques are only as good as the data they are trained with. However, data from previous designs may not be enough for AI to perform the necessary design operation and optimization. There is also real-time data. But real-time learning can be challenging because when something goes wrong we have to be able to debug, recover and repair the streaming data. Hence, my future research direction is to develop an AI-enabled electronic IC design smart database that will:

1. Learn the well-defined IC design parameter space: establish experimentally tested numerical libraries for this parameter space.
2. Create AI based Product Development Kit (PDK).
3. Explore AI generated device geometries for better performance, low power, low losses and new functionalities.
4. Demonstrate footprint reduction, auto-placement of devices while minimizing losses.
5. Accelerate of numerical simulation with deep learning based meta-models.
6. Create platform for AI assisted computational optical lithography.
7. Develop a new digital system based on probabilistic nanoelectronics, in contrast to conventional design of digital systems wherein the individual computing elements are deemed to work correctly all the time.

Awards & Honours

In 2009, Yeo was awarded the Public Administration Medal (Bronze) [PINGAT PENTADBIRAN AWAM (GANGSA)] by the President of Republic of Singapore for his outstanding efficiency, competence and industry and NTU's Nanyang Alumni Achievement Award in recognition of his exemplary achievements in research.

In 2012, Yeo received the Singapore Infocomm Technology Federation (SiTF) 2012 'Special Mention' Award under Emerging Technologies Category Awards for Singapore's Next Generation WiFi Chipset. He was conferred IEEE Fellow in 2016 for his contributions to low-power integrated circuit design.

Selected Patents

[1][2][3][4][5][6][7][8][9][10][11][12][13][14][15][16][17][18][19][20][21][22]

Selected Books

[23][24][25][26][27][28][29][30][31]

Selected Journal Papers

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Selected Conference Papers

[86][87][88][89][90][91][92][93][94][95][96][97][98][99][100][101][102][103][104][105][106][107]

Others

[108][109][110][111]

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Keywords

Yeo Kiat Seng; low-power integrated circuit (IC) design; RF/mm-wave; CMOS; VIRTUS; on-chip low-pass filter; VLSI/ULSI; system-on-chip (SoC); radio frequency; wireless communication