Multi-Level Inverter

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Multilevel inverter had been paid a lot of attention from the academia and research community in recent times due to its role in high and medium power applications.

pulse generation	cascaded unit	81	L-level	induction motor	ladder circuit	multilevel inverter
	pulse generation	n				

1. Introduction

Nowadays, multilevel inverters (MLI) play a major role in various power applications such as Electric Vehicle^[1], Photovoltaic systems^[2], Low-Power Loads^[3], Grid integration system^[4]. It is more attractive because of very low harmonic distortion, low number of drivers, absence of filters, low installation area, reduction in voltage stress and switching losses.

A generalized cascaded multilevel inverter is presented with nearest level modulation technique. The proposed converter is discussed with and without half bridge circuits^[4]. A new multilevel inverter with one DC source is presented for low power applications. The proposed inverter generates the output voltage eight times higher than the input voltage^[3]. In^[4], various configurations of MLI's were analyzed in terms of number of switching devices and modulation techniques. MLI are broadly classified into cascaded H Bridge, neutral clamped and flying capacitor topologies^[5].

Recently, for hybrid systems cascade multilevel inverters are applied. Many topologies are there to create the staircase voltages with higher levels with low devices count^[6]. A new MLI is designed to generate generate 27-level and fifty one level output voltages using constant voltage sources for resistive-inductive load^[7]. An inverter is designed using trinary DC sources and thirteen switches to generate 53 output levels with minimum THD of 1.15% ^[8]. A new switched source MLI is proposed which operates under both symmetric and asymmetric mode. The proposed inverter is designed with six power switches and two voltage sources^[9]. A new 81-level MLI is presented using two stage ladder circuits and the values of the dc sources are fixed by two different algorithms. The presented topology is tested with resistive and impedance load^[10]. A cascaded MLI is presented to generate 9, 15, 27, 33 and 39 output voltage levels at the load. It is observed that increase in number of voltage levels reduces the presence of harmonic content in load voltage and current waveforms. The proposed inverter is simulated in Matlab/Simulink and analyzed the total harmonic distortion for resistive and resistive-inductive load^[11]. Various configurations of symmetrical, asymmetrical and hybrid MLI's were synthesized in terms of number of switches,

capacitors, diodes utilized in the inverter circuit. As well, an analyzes is made in terms of THD generation and total standing voltages of all the configurations^[12]. Few drawbacks such as: switch count, voltage imbalance and number of DC sources are there in all the topologies^[13].

Multilevel inverter with minimum switch count is focused nowadays with higher voltage levels^[14]. Higher voltage levels are attained using cascaded H bridge MLI with isolated DC voltage sources. The switch count reduction is based on the design of basic unit. MLI with three phase is proposed with reduced power switches and has attained nine output voltage levels. The proposed structure is analyzed for various pulse width modulation (PWM) techniques. Total harmonic distortion is examined for all the PWM techniques^[15].

A new optimized structure of MLI is designed to create a rectangular type and circular type with a smaller number of switching components. A new switching technique is adopted and it is validated through simulation and experimental studies^[16]. A three phase cascade H bridge (CHB) inverter is proposed with discontinuous pulse width modulation which reduces switching losses and thus increases the lifetime of the switches. MLI also adopted with rotation scheme for even distribution of power in the switches^[17]. A trinary CHB MLI is proposed for solar power system with equal number of voltage levels.

For the control of active power and grid interaction, a modified second order integral control is applied^[18]. The space vector pulse width modulation scheme is being applied to the MLI for common mode voltage reduction^[19]. Two new MLI structures are designed and interfaced with PV system. Both the MLI structures consists of equal number of power switches and generates 9-level output^[20].

2. Issues in MLI with Low Device Count

In MLI, there are issues such as: Voltage unbalancing, gate pulse generation and circuit complexity. The major issues in various MLI topologies are discussed in Table 3. Some of the challenges are discussed below. In^[20] additional power stage is used, a transformer along with the inverter which increases the cost. Reactive power capability is absent in the structure proposed in^[20]. The design structure presented in^[21]^[22] requires a greater number of components for constructing higher number of levels. The design topology in^[23] uses bidirectional switches which increases the cost and size of the inverter. The inverter topology in^[24]^[25] utilizes more circuit components to generate higher output voltage levels. The reduction of harmonic content in the output load waveform is challenging and it is presented in^[26]. Inverter proposed in^[27] has higher total standing voltages. The presented topology in^[28]^[29] requires more circuits to achieve more output levels. A complex control is necessary inorder to design a bi-direction MLI^[30]. Voltage balance in the capacitor is challenging in the switched capacitor MLI with reduced switch count^[31]. Balancing the voltage in DC link needs high attention^[32]. The configuration presented in ^[33] utilizes more switches to generate higher number of voltage levels. In^[34], the basic structure of proposed system requires two bidirectional switches and it is used to generate 17-levels in the output via asymmetrical configuration. In order to increase the output levels by cascading the SLMLI unit or increasing the ladder structure that is 'm', the total voltage appeared across the switches S_x and S_y is becoming high and it increases the rating of

the devices. Furthermore, the switching frequency is high to generate desired output levels which increases switching losses.

Reference Paper Number	Type of MLI	Problems
35	Reduced switch MLI	Increase in input DC voltage sources.
36	Symmetric	Failure in finding out the PWM technique.
37	Symmetric	Failure in the implementation of medium and high voltage applications.
38	Asymmetric	Failure in designing the filter for harmonic reduction.
39	Asymmetric cascaded MLI	More number of switches are used.
40	Hybrid	Control technique is complex.
41	Symmetric and Asymmetric	 More blocking voltages due to bidirectional switches More switching losses Not applied for High voltage applications Cost Increases due to Bidirectional switches
42	Symmetric	More peak inverse voltage.
43	Cascaded switched diode MLI	Number of diodes is more.
44	Asymmetric	Requirement of more number of diodes due to high output voltage levels
45	Asymmetric	Switching scheme is more complex.
46	Asymmetric	Not possible for low frequency applications.
47	Reduced switch MLI	Low fault tolerant capacity.
48	Symmetric & Asymmetric	More number of diodes
49	Modularized MLI	Not suitable for high voltage applications.

Table 3. Issues in MLIRS.

Reference F	raper Type	e of MLI	Problems umber of
[<u>37</u>] 50	Symr Asy	netric and More swi mmetric level.	ches to be turned on to generate a voltage h voltage

applications. In ^{[38][39]}, a multileventivenents designed using asymmetrical voltage sources to generate more output voltages levels with increase in the number of switches. A hybrid MLI designed with complex control technique and it is presented in ^[40].

In^[41], the proposed system is used to generate 9-levels in the output with four dc sources, eight switches and four diodes. While extending the output voltage levels, more units are added and thus conduction and switching losses are more. In addition to increase in switching loss, stress across the switch is increasing.

Circuit proposed in^[42] consists of single source and double sources configuration to build multi levels in the output by connecting the sources in series and parallel. For this configuration there is a possibility of short circuit of DC sources while turning on the sources and voltage stresses between the switches is high. A Cascaded switched diode MLI is designed utilizing more number of diodes^[43].

In^[44], proposed cascaded switched diode structure consists of two stages. First stage contains dc sources, switch and diode. The second stage is an H-bridge inverter, in order to increase the multilevel in the output, number of units in the first stage is increased and thus large number of switches and diodes are required.

Conventional diode clamped and capacitor clamped multilevel inverters^[45] are modified by adding single phase full bridge inverter. This proposed system reduces the number of switches but the requirement of diodes and capacitors are increased compared to the conventional inverters.

Significant factors of inverter design using Asymmetric voltage sources presented in^[46] is identified and tabulated in <u>Table 2</u>. As well, few of the challenges in the reduced switch $MLI^{[47]}$, Asymmetric $MLI^{[48]}$ and modularized $MLI^{[49]}$ were identified and listed in <u>Table 2</u>.

In^[50], 9-levels of output voltage are generated using 12 numbers of switches and 4 number of dc sources. In order to construct each level of output waveform, six switches are required to be turned on at an instant and thus switching losses are increasing. A 9-level symmetric and 31 level asymmetric inverter were simulated using a smaller number of voltage sources^[51]. Using large number of switches, a symmetric MLI topology is designed and experimented in ^[52]. Also various topologies of MLI were designed using optimal number of switches^{[53][54][55][56][57]}.

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