Switched-Biasing Techniques for CMOS VCO

Subjects: Engineering, Electrical & Electronic

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A voltage-controlled oscillator (VCO) is a key component to generate high-speed clock of mixed-mode circuits and local oscillation signals of the frequency conversion in wired and wireless application systems. In particular, the recent evolution of new high-speed wireless systems in the millimeter-wave frequency band calls for the implementation of the VCO with high oscillation frequency and low close-in phase noise. The effect of the flicker noise on the phase noise of the VCO should be minimized because the flicker noise dramatically increases as the deep-submicron complementary metal-oxide-semiconductor (CMOS) process is scaled down, and the flicker corner frequency also increases, up to several MHz, in the up-to-date CMOS process.

Keywords: CMOS ; voltage-controlled oscillator ; switched-biasing ; flicker noise ; phase noise ; current source ; figure-of-merit

1. Introduction

A voltage-controlled oscillator (VCO) is a key component in a frequency synthesizer that generates local oscillator (LO) signals for frequency conversion in a radio-frequency (RF) transceiver[1][2][3]. A VCO-based readout circuit, which is that the output voltage of the sensing core is applied to the node of the VCO tuning voltage, has merit to achieve a low sensitivity level and a high signal-to-noise ratio compared to the amplifier-based readout circuit[4][5]. In addition, high integration and low power consumption of the VCO-based readout circuit are advantageous for implementing a large-scale sensor array [6][7]. Radar sensors that monitor the change of electromagnetic-wave between the transmitted and received signals generated from the VCO remotely measure the distance, velocity, and vital-signs in real time[8][9][10]. Various sensors using VCOs require low phase noise characteristics in VCOs [11][12][13]. The frequency synthesizer such as the phase-locked loop (PLL) is conventionally used to reduce the phase noise, but the noise characteristics still remain at the output signal of the frequency synthesizer because the loop bandwidth of the PLL in the synthesizer is generally determined to be between 100 and 500 kHz[14][15].

A complementary metal-oxide-semiconductor (CMOS) process is a standard fabrication technology to implement electrical circuits; it can integrate control, logic, analog, and RF circuits into a single-chip system[16]. Moreover, the recent CMOS device designed in the several nanometer-scale shows competitive performances in transconductance (g_m) and minimum noise figure (NF_{min}), compared to the compound semiconductor device[17]. However, the transistor device implemented in the up-to-date CMOS process exhibits an increase in the flicker noise, which intrinsically depends on the physical structure of the channel and the flicker corner frequency, where the magnitudes of the flicker and white noises present equal increases up to several MHz or more[18][19]. The flicker noise is called “1/f noise” because the noise is increased as the frequency in the channel decreases[20]. The nanometer-scaled CMOS technology has advantages such as high integration, low power consumption, and high operating frequency, but it has the disadvantage of noise deterioration in the low-frequency band owing to the increase in the flicker noise[14].

The reduction in the flicker noise is a major issue in VCO design using the CMOS process because the phase noise of the VCO is mainly determined by the noise in the low-frequency region[21]. Many studies have been conducted to improve the reduction in the CMOS VCO phase noise performance caused by the flicker noise. Biasing techniques for core transistors have been widely used to prevent the degradation of the VCO phase noise by the flicker noise of the oscillator core transistors[22][23]. A VCO using core transistors biased at class C operation is a representative technique that reduces the contribution of the flicker noise effect from the core transistor at the output[24][25][26]. A resonant filter at the second harmonic also minimizes the noise effect from the core transistors, but the large chip size and the tuning range limit cause other issues in the design of the VCO using this technique[27]. The increase in the chip area can be reduced by implementing the filter using the common-mode resonance of the LC tank in a cross-coupled LC oscillator, although the issue of the tuning range limit cannot be solved[15][28][29]. The performance degradation by the noise of the core transistors is reduced by these techniques, but the contribution of the flicker noise caused by the current source, which is used to constantly supply the DC bias current in the core transistors, remains in the output characteristics of the VCO. The flicker

noise by the current source dramatically increases the close-in phase noise of the VCO owing to the nonlinear characteristics of the VCO[30]. A simple method to reduce the effect of the flicker noise from the transistors constituting the current source is to design the VCO using only voltage biasing, that is, without using any current sources[14][31]. However, the core current of the VCO can easily deviate from the designed value depending on the power supply variations when current biasing is not used. It can also be observed that the oscillator becomes more sensitive to ground noise[21]. A switched-biasing technique has been proposed to reduce the flicker noise effect of the current source based on the periodic behavior of the differential VCO[32][33]. The up-conversion behavior of the flicker noise of the current source can be fundamentally eliminated using the switched-biasing technique, which is based on the periodic operation of the differential VCO[34].

2. Switched-Biasing Technique

As the deep-submicron CMOS process is scaled down, the low-frequency noise (especially the flicker noise) of the MOSFET becomes more important in the design of CMOS RF transceivers. It has long been known that the flicker noise is generated in a variety of homogeneous semiconductor bulks and is observed in various devices, such as a vacuum tube, diode, and MOSFET[35][36]. Various research works have been conducted to identify the cause of the flicker noise and to clearly understand its characteristics clearly [32][33][34][35][36][37][38][39][40][41][42][43]. To predict the flicker noise phenomenon generated in MOSFETs, Hooge published a carrier mobility fluctuation (CMF) model, in which the flicker noise is caused by the mobility fluctuation of free carriers in the device[37]. McWhorter suggested a carrier number fluctuation (CNF) model, where the low frequency noise of the MOSFET is generated by the fluctuation in the number of charge carriers in the device[38]. The two presented models were useful for understanding the physical mechanism of the flicker noise, but their limitation is that they can only be applied to the long-channel devices. The flicker noise in short-channel devices is mainly considered to be due to the random telegraph signal (RTS) noise generated by the $Si-SiO_2$ interface because as the size of the devices is scaled down, the device operation is predominantly represented by the movement of each charge carrier[39][41][44].

Research on reducing the intrinsic flicker noise of MOSFETs began in the early 1990s. Bloom and Nemirovsky first suggested that the flicker noise of the MOSFET could be reduced by cycling between inversion and accumulation of the device[40]. They explained that the device noise in the on-state can be reduced when the off-state exists before the on-state. Dierickx and Simoen revealed that the flicker noise reduction by inversion-to-accumulation cycling is related to the emptying of traps at the interface that generates RTS noise[41]. Based on the principle of inversion-to-accumulation cycling, Gierkink et al. proposed a switched-biasing technique[32]. Figure 1 shows the operating principle of the switched-biasing technique[33]. The “operational state” in Figure 1 means that the MOSFET operates at the inversion state, to facilitate the flow of current between the drain and the source. The drain–source current does not flow at the “rest-state” of the MOSFET because the bias voltage at the gate is lower than the threshold voltage of the device. A reduction in the flicker noise can be expected by the periodic operation between the two states of the device and is verified with a simple mathematical analysis. Assuming a duty cycle of 50%, the drain–source current of the MOSFET by the switching operation can be expressed as the multiplication of the flicker noise and a square-wave signal $m(t)$ with the duty cycle,

where ω_{sw} is the angular frequency of the switching operation. Because the power spectral density (PSD) of the noise in the low-frequency band is determined by the convolution of the DC component of $m(t)$ and the flicker noise, the switched-biasing technique can decrease the PSD by 6 dB compared to the constant-biasing technique. In addition, several studies have confirmed that the flicker noise is further reduced when the transistor is sufficiently turned off (i.e., deep accumulation). This reduction is known to be caused by the elimination of the long-term-memory effect associated with the flicker noise[32][33][44] The analysis of the operating characteristics and principle shows that the PSD due to low-frequency noise depends on the bias state at the time and the bias history in a periodic operation [44]. This phenomenon was verified in both NMOS and PMOS because the carrier type does not affect the operating principle[43].

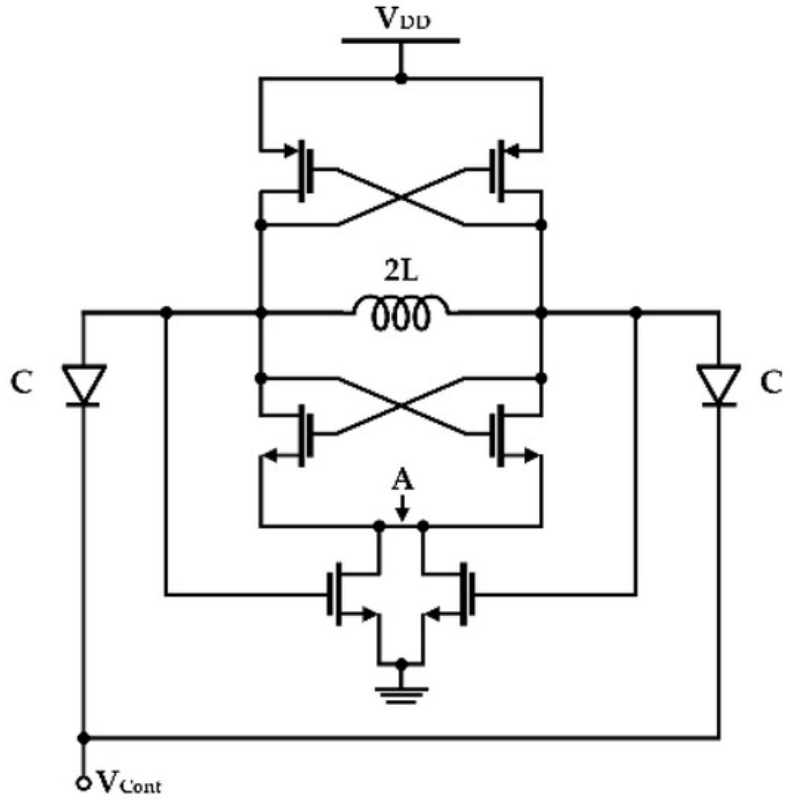

Figure 2. Schematic of a CMOS LC-VCO with the switched-biasing technique to the current source (reproduced with permission from the author, RF CMOS low-phase-noise LC oscillator through memory reduction tail transistor; published by IEEE, 2004)[34].

The characteristics that the current source modulated by the switched-biasing technique is effective in improving the phase noise of a VCO was proved using a theoretical analysis based on a mathematical model[47]. The proposed theoretical analysis is based on the impulse sensitivity function (ISF) theory, which can explain the phase noise contribution depending on the output voltage swing of the VCO. The proposed analysis in Figure 3 shows that the phase noise of a VCO can be greatly improved by additionally injecting the bias current to the VCO core transistors at the time when the voltage swing of the VCO is maximized or minimized. This phenomenon is based on the fact that the time when the output voltage of the VCO becomes the maximum or minimum has the minimum sensitivity to the phase shift[47] . Figure 3b shows that the phase noise of the VCO can be minimized by the modulation signals of $2f_0$ in the current source compared to the fixed-biasing current source. It is caused that the bias currents of the cross-coupled transistors in the VCO using the switched-biasing current source are limited at a time of high phase-shift sensitivity and supplied at a time of low phase-shift sensitivity. The currents I_{d1} and I_{d2} supplied from the switched biasing current source are not supplied at the highly sensitive time in the phase noise where the output voltages $V_{o,n}$ and $V_{o,p}$ are crossed. Based on physical and theoretical interpretations, it can be verified that the switched-biasing technique improves the phase noise of the VCO by modulating the current source.

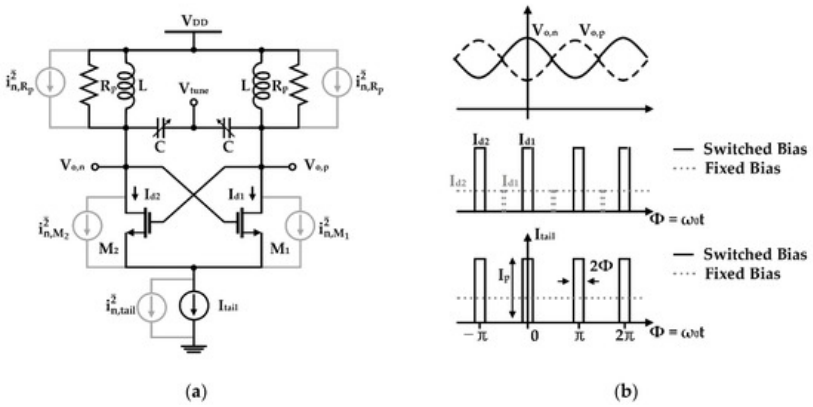

Figure 3. Analysis of VCO characteristics depending on the pulse modulation of the current source using the impulse sensitivity function theory: (**a**) schematic of the differential LC-VCO; (**b**) conceptual waveforms of the output voltages and drain currents of the VCO and the bias current by the pulse-modulated current source (reproduced with permission from the author, Tail current-shaping to improve phase noise in LC voltage-controlled oscillators; published by IEEE, 2006)[47].

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