SiC Trench MOSFETs' Reliability under Short-Circuit Conditions

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MOSFETs exhibit different failure modes at different DC bus voltages. For double trench SiC MOSFETs, the failure modes are gate fault at lower DC bus voltage and thermal runaway at higher DC bus voltage, while the failure modes for asymmetric trench SiC MOSFETs are soft failure and thermal runaway, respectively. The short-circuit withstand time (SCWT) of the asymmetric trench MOSFET is higher than that of the double trench MOSFET. The thermal and mechanical stresses inside the device during short-circuit test are simulated to explore the failure mechanism and reveal the impact of device structure on device reliability. Finally, a post-failure analysis was performed to verify the root cause of the equipment failure.

SiC trench MOSFET | short-circuit failure mechanism | failure analysis

1. Introduction

Over the past few decades, wide-bandgap semiconductors like SiC have become more attractive compared to traditional silicon devices due to their high breakdown field, high thermal conductivity, and wide bandgap [1][2]. By now, iC devices such as Schottky diodes have been rapidly developed and are widely used commercially [3][4]. However, the short-circuit performance of SiC MOSFETs is still poor compared to Si-IGBTs. Due to their smaller area and higher power density, SiC MOSFETs have higher junction temperatures than Si-IGBTs and tend to suffer from thermal runaway [5][6][7][8]. In addition, the poor interface state problem of SiC MOSFETs can also lead to gate reliability issues, causing the device gate failure [9][10].

As SiC material growth and device fabrication technologies have evolved, the structure of SiC MOSFETs has become increasingly sophisticated. Today, various commercial SiC MOSFETs with planar and trench gate structures from different manufacturers are available [11][12]. Compared to SiC planar gate MOSFETs, trench gate MOSFETs have higher power density and lower conduction resistance [13]. Although SiC trench MOSFETs have many advantages, their reliability needs further research due to the defects introduced during manufacturing process [14]. First, the inhomogeneity of oxidation during gate formation makes the oxide thickness at the sidewall and trench bottom inconsistent. The oxidation inconsistency increases the SiO2

/SiC surface roughness, and leads to local electric field concentration at the rough point. Hence, more charges are injected into the gate oxide, increases the charge through the gate oxide, shortening the time to dielectric breakdown [15][16]. Otherwise, threading dislocations (threading screw dislocations (TSDs) and threading edge dislocations (TEDs)) can cause significant leakage points in the device, which can severely degrade the

performance of the SiC device [17][18]. The second issue is the infamous interface state problem. In addition, SiC devices tend to be operated under high voltage conditions, which makes the gate oxide layer bear a high electric field. In response, different shielding methods have been proposed, such as double trench MOSFETs (DT-MOSFETs) and asymmetric trench MOSFETs (AT-MOSFETs) [19][20]. The short-circuit failure modes of DT-MOSFETs have been reported in some detail [21][22], while the short-circuit reliability of AT-MOSFETs has been less studied. A comparison of the two devices' short-circuit reliability has been reported [23], but it focuses more on the safe operating region and failure prediction regarding the device failure mode. The difference in the internal thermal and mechanical stress during the short-circuit process related to the difference in device structures has not been addressed.

2. Device Structure and Experiment Setup

2.1. Device Structure

The short-circuit reliability of two 1200 V SiC commercial power trench MOSFETs manufactured by Rohm and Infineon, respectively, have been chosen as the devices under test (DUTs) [24][25]. The main electrical parameters of the devices have been listed in **Table 1**. **Figure 1** shows the cell structure of two devices. The structure parameters of the devices have been obtained by SEM and FIB, as shown in **Figure 2**. The doping concentrations of the device have been obtained by fitting the device characteristics (transfer curve, output curve, breakdown voltage, etc.) by the numerical simulation.

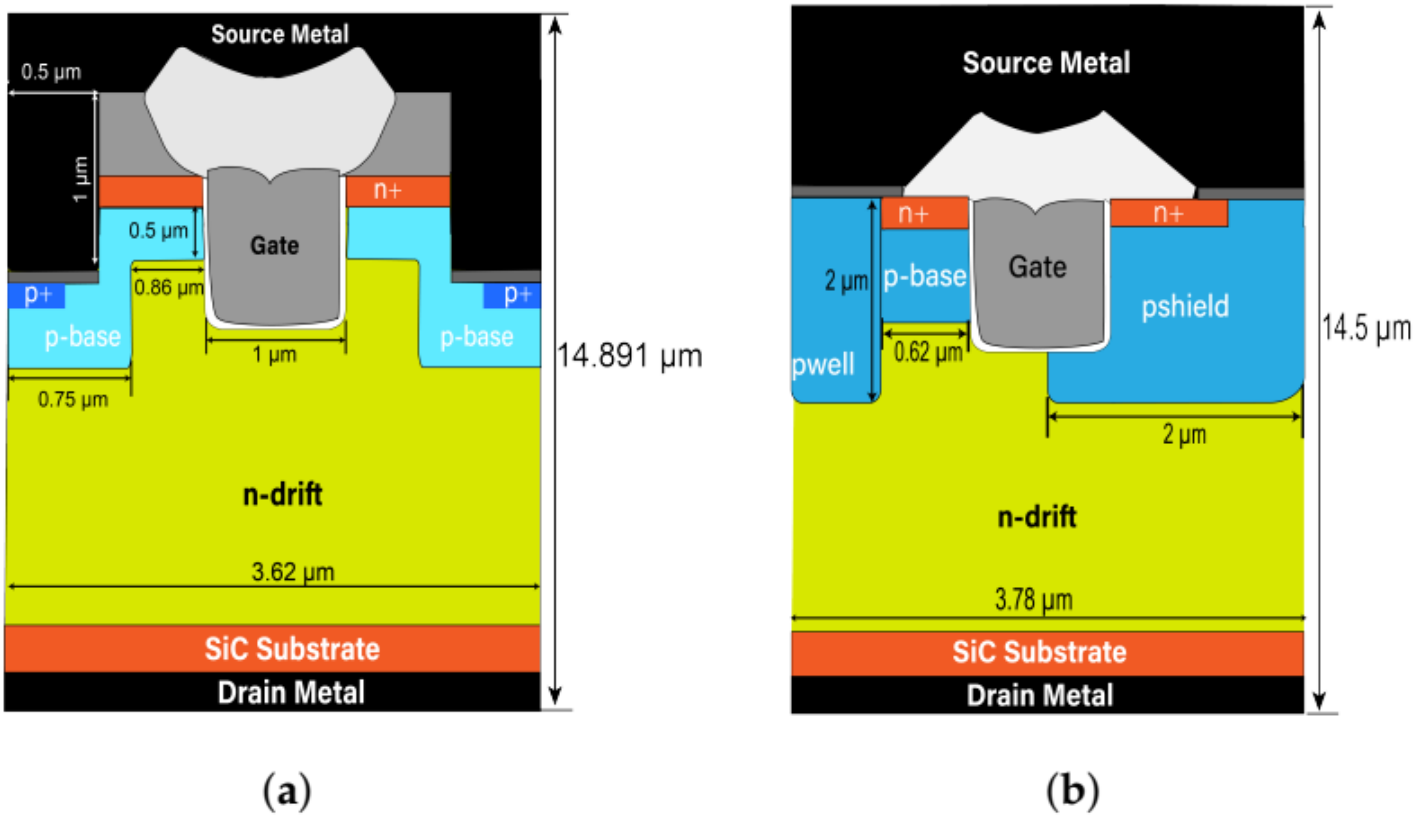

Figure 1. Cross-section images of the two trench MOSFETs. (**a**) DT-MOSFET. (**b**) AT-MOSFET.

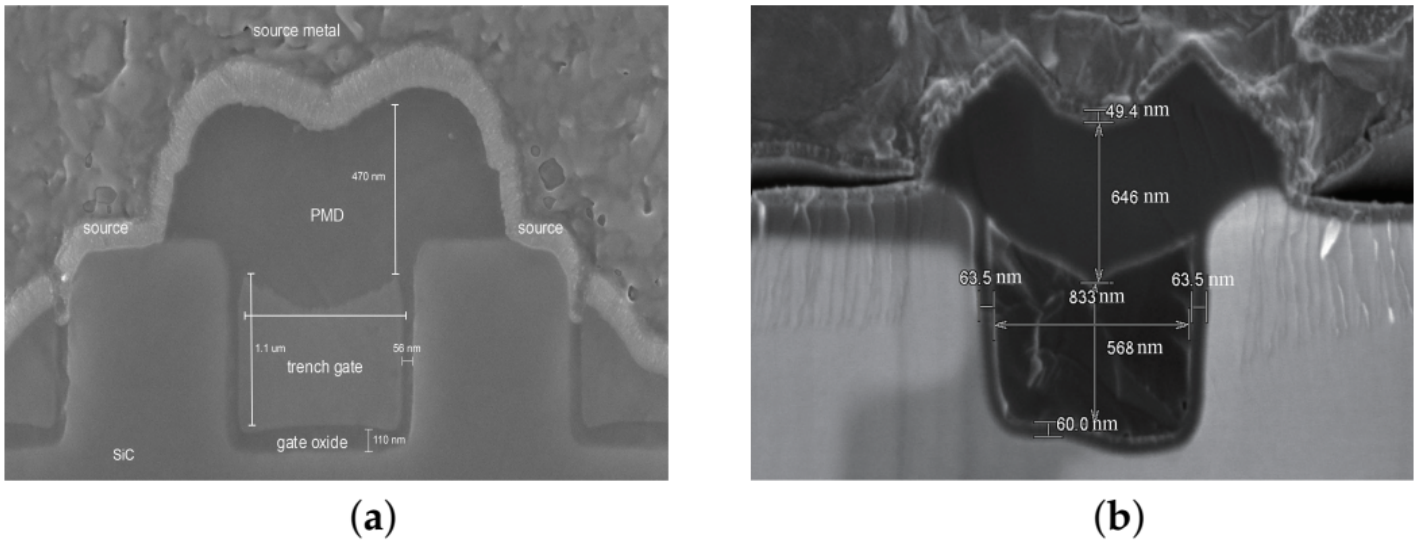

Figure 2. Cross-section images of the two trench MOSFETs by FIB and SEM. (**a**) DT-MOSFET. (**b**) AT-MOSFET.

Table 1. Device rated parameters.

Rated Parameters	Rohm (DT-MOSFET)	Infineon (AT-MOSFET)
V_{DS}	1200 V	1200 V
$R_{DS(on)}$ (Typ.)	160 mΩ	90 mΩ
I_D	17 A	26 A
Power dissipation	103 W	115 W
Drive Voltage	0 V/18 V	0 V/15–18 V
Junction temperature	175 °C	175 °C
Active area	3.1378 mm^2	3.0751 mm^2
Package	TO-247N	PG-TO247-3
Orderable Part Number	SCT3160KLGC11	IMW120R090M1HXKSA1

2.2. Experiment Setup

Figure 3 shows the short-circuit test circuit schematic diagram and the photograph of the test platform. To provide sufficient energy during the short-circuit, C1 consisted of six 50 μF/1200 V capacitors [26]. In order to avoid device catastrophic failure, an IGBT [27] was employed as the solid-state circuit breaker. Initially, both the IGBT and the DUT were kept off. At first, S1 was turned on and the capacitor C1 was charged to a high voltage via a DC power supply. Afterwards, S1 was turned off and the short-circuit stress was applied to the DUT. The short-circuit pulse width was varied by controlling the gate signals of the IGBT and the DUT. The short-circuit capability of the device can be quantified by the short-circuit withstand time (SCWT), reflecting the maximum short-circuit time that the device can tolerate. After every single test, the device was cooled down to room temperature before the next test started to prevent the heat accumulation inside the devices.

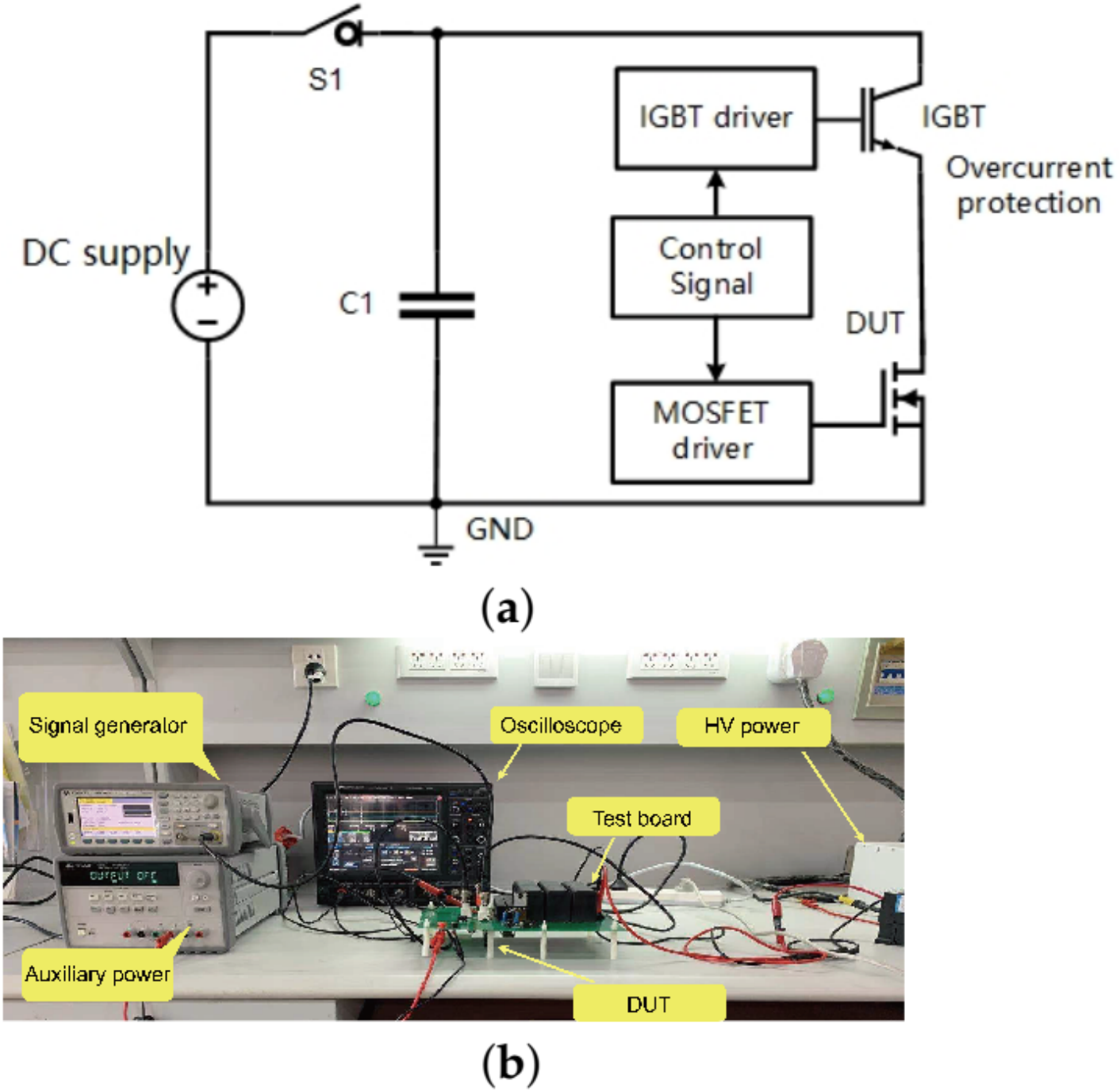

Figure 3. Circuit schematic diagram: (**a**) Simplified schematic of the short-circuit test. (**b**) Photograph of the test platform.

3. Experiment Results

3.1. DT-MOSFET

Figure 4 shows typical experimental short-circuit waveforms of SiC DT-MOSFETs with VDC = 300 V and VGS = 18 V/−3 V. When the device is turned on, internal parasitic parameters of the device and the test board cause a brief

overshoot on VGS and VDS. However, this overshoot does not affect the following short-circuit process [26]. The short circuit pulse width tsc was gradually increased to 28 µs until the device reached the failure point, accompanied by a peak current value of 125 A and a VGS drop of 2.5 V. The anomaly only showed on the gate voltage waveform, manifested as a sudden increase of VGS (from −3 V to 0 V) after the device has been turned off for 7 µs, whereby the drain-source voltage still maintained to DC bus voltage. This means that the gate and source terminals are shorted, while the drain-source body diode still has blocking capability. The measured waveforms indicate the gate failure mode [10][27][28]. The same result was demonstrated in the subsequent electrical inspection of the three terminals, as shown in **Table 2**.

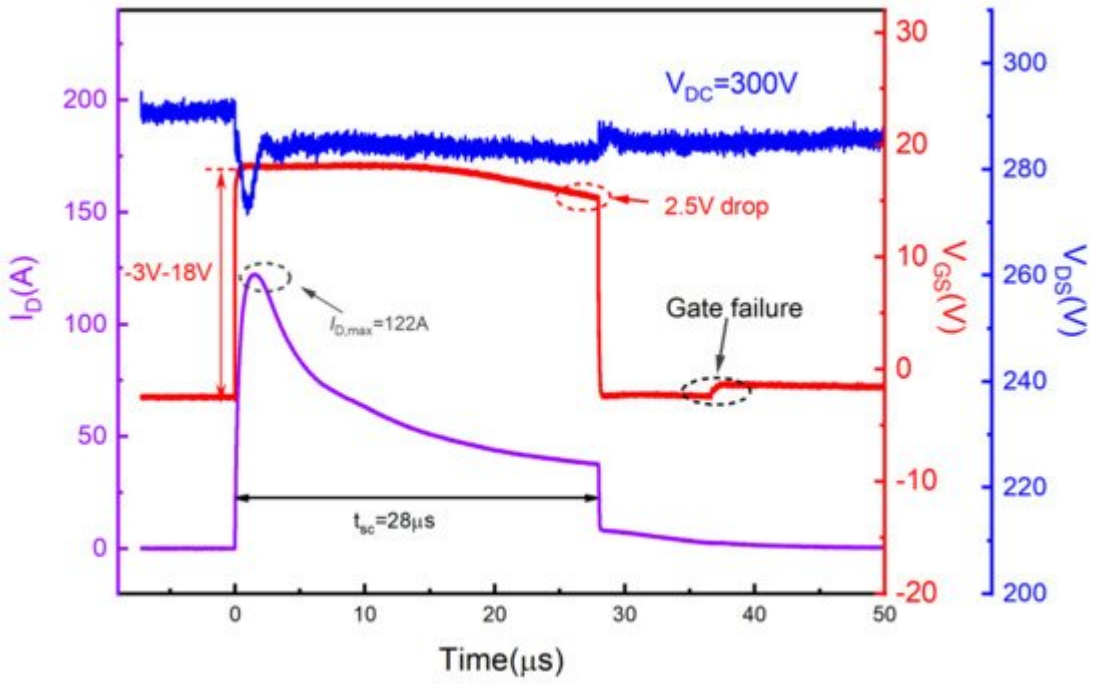

Figure 4. Short-circuit failure waveforms for the SiC DT-MOSFETs at 300 V DC bus voltage.

Table 2. DT-MOSFET: Measured resistances between electrodes before and after tests.

Device State	R_{GS} (Ω)	R_{DS} (Ω)	R_{GD} (Ω)
fresh device	>100 M	1.529 M	>100 M
V_{DS} at 300 V	8.6	>100 M	84 k
V_{DS} at 600 V	3.36	3.05	2.36

Figure 5 shows the short-circuit waveforms of SiC DT-MOSFETs measured before the failure (a) and at the failure (b), when increasing the bus voltage to 600 V. Higher DC bus voltage leads to higher power dissipation, causing the SCWT to decrease to 7 µ

s. When the device fails, the peak current value is about 135 A, accompanied by the VGS drop of about 1 V. It can be seen from **Figure 5**b that a significant trail current appears after the device is turned off, climbing up to 39 A. High junction temperature caused by high power consumption can significantly increase the carrier density. Therefore, the device cannot be completely shut down at the end of short-circuit operation [29]. The hole current is

the main cause of tail currents. Due to the existence of the tail current, more heat is generated, forming a positive feedback. If the tail current exceeds the threshold current to trigger the parasitic BJT, the hole density and the junction temperature will increase further and finally lead to thermal runaway [30]. As listed in **Table 2**, the resistance between the three terminals (RGS, RGD, and RDS) after the short-circuit test became quite low, revealing that all electrodes were shorted.

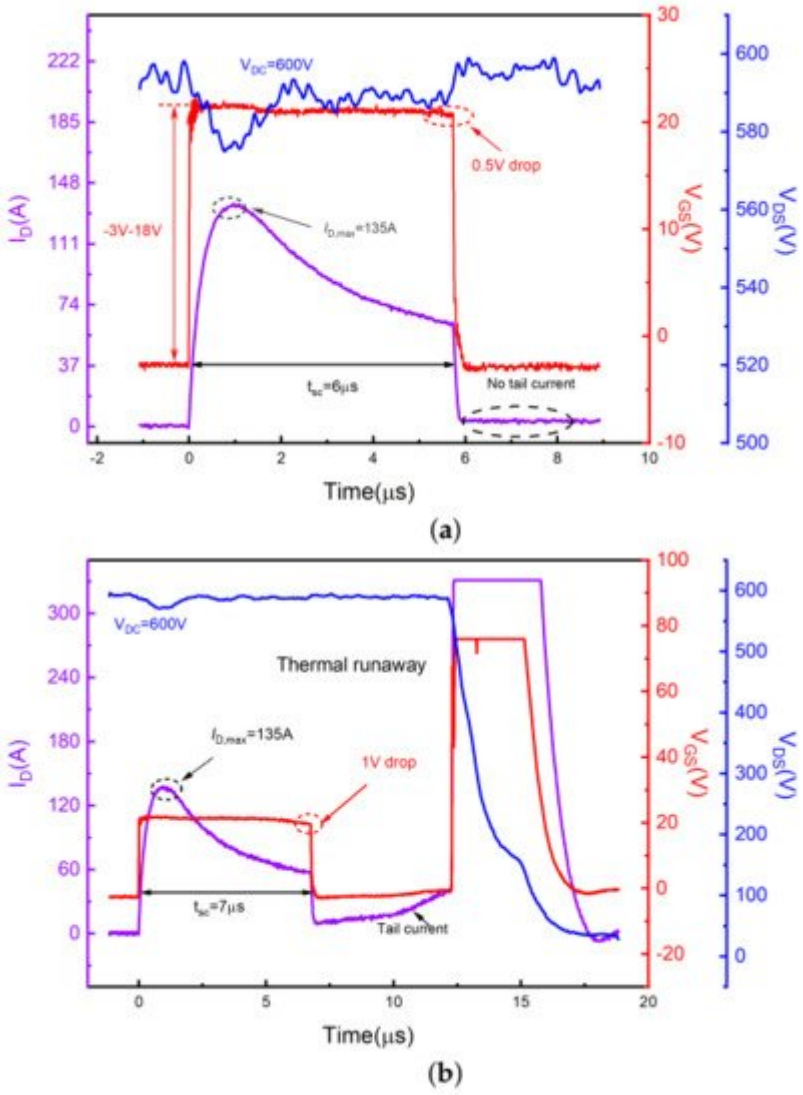

Figure 5. Short-circuit waveforms for the SiC DT-MOSFETs at 600 V DC bus voltage. (**a**) Last waveforms before failure and (**b**) failure.

3.2. AT-MOSFET

Figure 6 shows typical experimental short-circuit waveforms of SiC AT-MOSFETs at 300 V DC bus voltages, and gate bias was set as VGS = 18 V/−3 V. Under the same conditions, the SiC AT-MOSFET shows better short-circuit performance than the DT-MOSFET (35 μs for AT-MOSFET, 28 μs for DT-MOSFET). However, the longer short-circuit time leads to more serious device damage. After withstanding a 35 μs short-circuit pulse, the device is no longer able to operate normally. First, the short-circuit current

drops to a dozen amps and shows an abnormal upward trend. In addition, the gate voltage is 9 V/−2 V even external 18 V/−3 V is applied. This indicates that a leakage path is formed between the gate and source, but they are not completely shorted, which is referred to as the soft failure. Devices have been previously reported to fail at low bus voltages due to gate-source SiO2 rupture [33]. Therefore, it can be inferred that the gradual accumulation of dielectric layer damage in AT-MOSFETs under prolonged short-circuit stress may be the root cause of soft failure. The device body diode is still able to carry 300 V. The results of the subsequent electrical inspection of the three terminals are shown in **Table 3**.

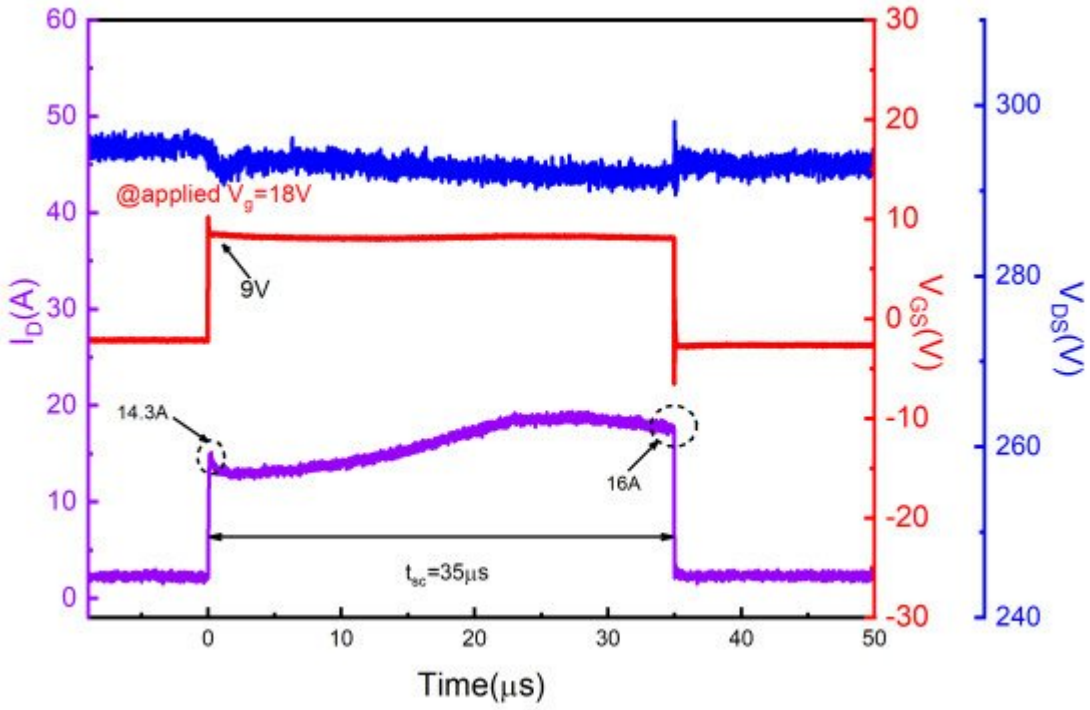

Figure 6. Short-circuit failure waveforms for the SiC AT-MOSFETs at 300 V DC bus voltage.

Table 3. AT-MOSFET: Measured resistances between electrodes before and after tests.

Device State	R_{GS} (Ω)	R_{DS} (Ω)	R_{GD} (Ω)
fresh device	>100 M	1.529 M	>100 M
V_{DS} at 300 V	6.86	0.128 M	>100 M
V_{DS} at 600 V	3.36	3.12	2.54

Figure 7 shows short-circuit waveforms of SiC AT-MOSFETs at 600 V DC bus voltages, and gate bias was set as VGS = 18 V/−3 V. At higher bus voltage, the device is subjected to higher power dissipation and the AT-MOSFET exhibits a thermal runaway mode after a 8.5 μs SC pulse. The performance is slightly better than that of DT-MOSFETs, but it is somewhat different from the thermal runaway mode of DT-MOSFETs. First, the thermal runaway of the AT-MOSFETs does not occur after the device is turned off, but during the period when the short-circuit stress is applied. A comparison with the last waveforms measured before failure shows that the current increases during the short-circuit pulse. For example, the drain current increased from 66 A to 78 A at 7 μs. This indicates that a trailing current has occurred during the short-circuit pulse. As the junction temperature increases

further, the current value is sufficient to trigger the parasitic BJT before the device shuts down. Compared to the DT-MOSFETs, the higher power level of the AT-MOSFET results in a higher peak current than the DT-MOSFETs, making the junction temperature rise faster, thus causing the thermal runaway mode to be triggered before the device is turned off. The second point is that the gate-source voltage of the AT-MOSFETs exhibites anomalies during the short-circuit pulse. There is a gate voltage drop of about 4 V near the point of failure, indicating that a high leakage current is flowing across the gate resistance. This indicates that the gate degradation occurs also. However, the junction temperature rises rapidly due to the higher bus voltage, so that there is not enough time for the gate to be damaged seriously before the thermal runaway occurs. The electrical characteristics in **Table 3** also shows that all three terminals of the device are shorted together.

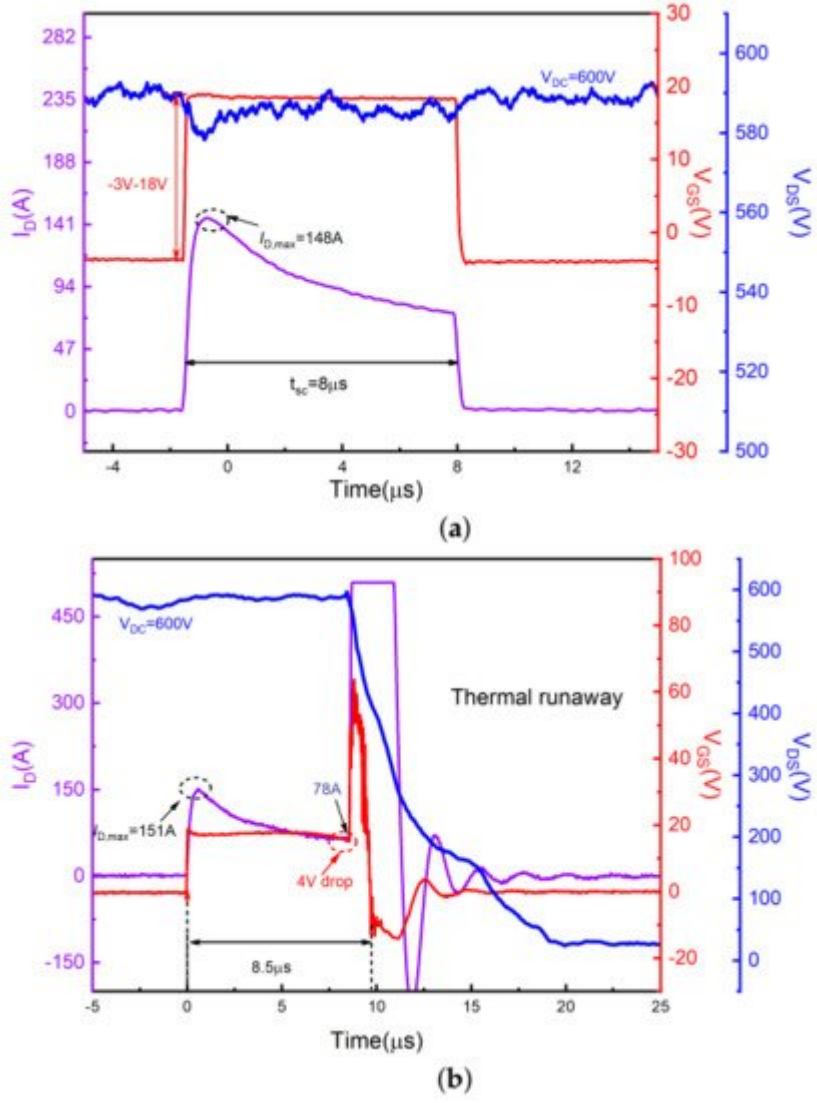

Figure 7. Short-circuit waveforms for the SiC AT-MOSFETs at 600 V DC bus voltage. (**a**) Last waveforms measured before failure and (**b**) at failure.

The results of SCWT and extracted Pmax comparison between DUTs are shown in **Figure 8**. The maximum power dissipated in the short-circuit test is higher because the AT-MOSFETs has a higher current rating than the DT-

MOSFETs. However, the survival time of DT-MOSFETs at different bus voltages are shorter than that of AT-MOSFETs, which needs further study.

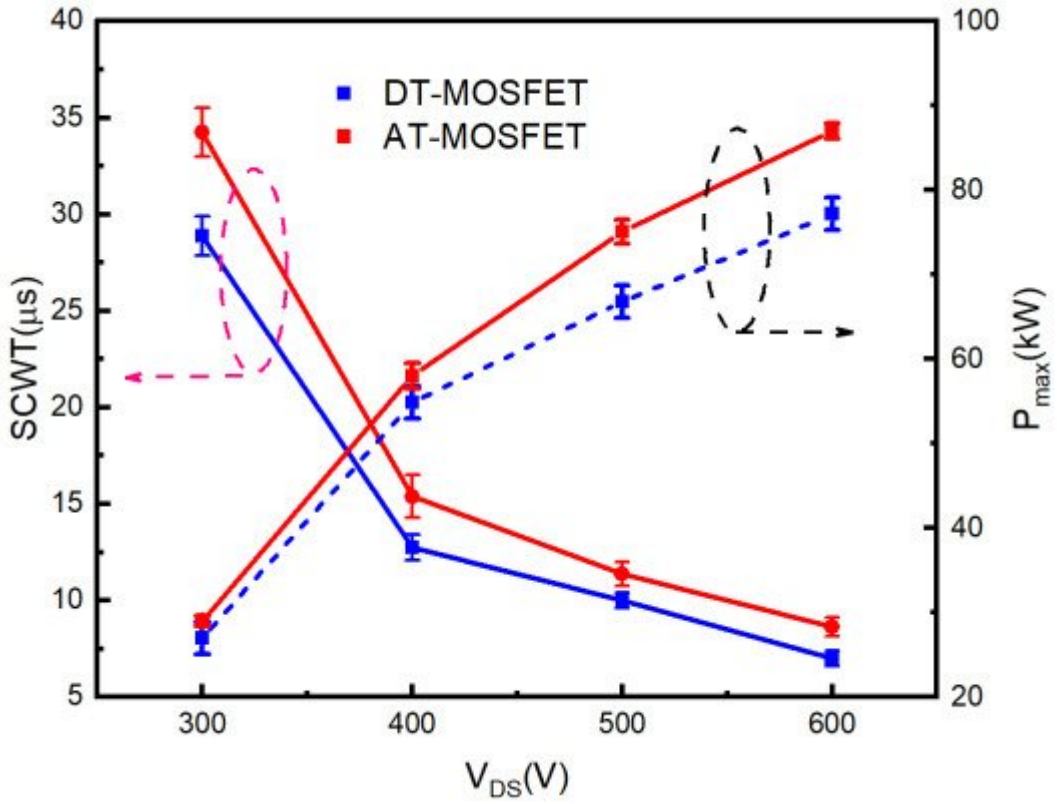

Figure 8. SCWT and Extracted Pmax comparison of different DUTs under different conditions.

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