Profiling the Cycling-Induced Oxide Trapped Charge

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NAND Flash memories have gained tremendous attention owing to the increasing demand for storage capacity. This implies that NAND cells need to scale continuously to maintain the pace of technological evolution. Even though NAND Flash memory technology has evolved from a traditional 2D concept toward a 3D structure, the traditional reliability problems related to the tunnel oxide continue to persist.

Keywords: NAND Flash memory ; endurance ; reliability ; oxide trapped charge

1. Introduction

The emergence of NAND Flash memories has revolutionized the data storage industry over the last few decades. NAND Flash devices are used in a wide range of applications in everyday consumer electronics such as laptops, tablets, and smart wearable devices. The first NAND-structured cell was invented in 1987 by Masuoka et al. [1] at Toshiba Corp. Since then, several improvements have been proposed to lower the power consumption of these cells and to enable the contents of the entire chip to be erased at once [2][3][4][5][6][7]. More recently, its application range has been expanded such that it has become the main storage element, in that solid-state drives (SSDs) are gradually replacing hard disk drives (HDDs) [8][9]. Furthermore, it is increasingly adopted for enterprise-class storage systems. As a result, the size of NAND cells has aggressively shrunk to continuously promote this evolution. However, the ever-shrinking dimensions of the NAND cell create additional challenges in terms of the endurance and retention characteristics, such as random telegraph noise (RTN) fluctuations of the threshold voltage (V_T) [10][11][12], charge trapping/detrapping mechanisms [13][14][15], electron injection statistics [16][17], and V_T distribution widening due to parasitic coupling effects [18][19].

Three-dimensional (3D) NAND Flash memories can be considered as a breakthrough to continue to deliver increasing bit density and reduce the bit cost [20]. 3D NAND Flash technology can utilize either floating gate (FG)- or charge trapping (CT)-type cells. Most of the 3D NAND reported to date are CT-type, owing to the simpler fabrication process [21]. The 3D NAND array architecture can be categorized into the following two classes depending on the direction of channel, as schematically shown in **Figure 1** : vertical gate 3D NAND architecture, which was proposed by Samsung Electronics in 2009 [22]; and vertical channel 3D NAND architecture. There are two main cell structure types that use vertical channels, namely bit cost scalable (BiCS), which was proposed by Toshiba Corp. in 2007 [23][24], and terabit cell array transistor (TCAT), which was developed by Samsung Electronics in 2009 [25]. TCAT subsequently evolved into V-NAND architecture, which has 32-stacked word line (WL) layers [26][27][28]. The industry has moved beyond 12x-stacked WL layers and achieved a 17x-stacked V-NAND [29][30]. As the memory industry transitions from planar to 3D scaling, traditional device reliability issues must still be considered. The Fowler Nordheim (FN) tunneling mechanism is commonly used in both planar and 3D NAND cells during programming and erasing (P/E) operations [31]. This mechanism leads to the formation of trap states in the tunneling oxide, and thus degrades the oxide reliability. Therefore, overcoming the reliability problems related to the oxide trap is critically important for the development of future advanced NAND Flash memories.

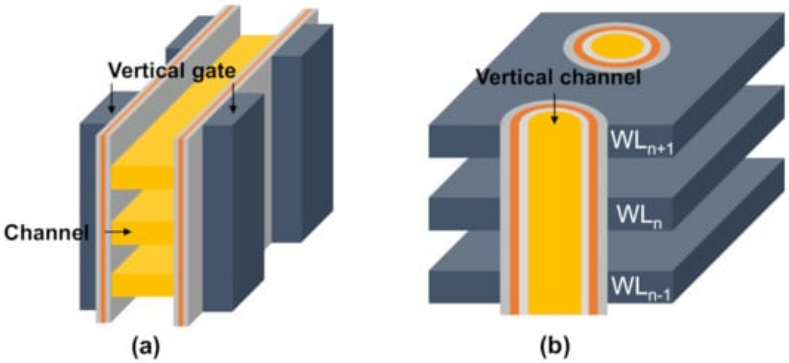

Figure 1. Schematic diagrams of 3D NAND architecture: (**a**) vertical gate and (**b**) vertical channe

2. Shift in the Midgap Voltage

Generally, the midgap voltage (ΔV_{MG}) during P/E operations is described by a set of two components [32]: the first is the electrostatic shift (ES) that is caused by the creation of oxide trapped charges (Q_T), and the other is the tunneling shift (TS) that is related to the change in the number of floating-gate charges (Q_{FG}). Notably, these two components mutually influence each other. The former deforms the tunneling barrier for P/E operations and thus reduces the number of storage electrons. ΔV_{MG} can be expressed as the sum of these two components.

$$\Delta V_{MG} = \frac{Q_T}{C_i} + \frac{\Delta Q_{FG}}{C_{IPD}} \quad (1)$$

(1)

where Ci and CIPD are the tunneling oxide and the interpoly dielectric capacitance, respectively.

Several approaches have been proposed to separate the ES and TS values from ΔV_{MG} . The first category of methods is based on indirect measurements. For example, the ΔV_{MG} in the programming and erasing states combined with tunneling-based modeling is commonly monitored to extract the Q_T distribution from Q_{FG} in NAND Flash memories. Q_{FG} has been presented by a sheet charge located at fixed distance from the channel in the majority of the literature [32][33][34]. Under this assumption, the tunneling current is calculated straightforwardly along the direction perpendicular to the channel by using the Wentzel–Kramers–Brillouin (WKB) approximation, as schematically shown in **Figure 2** a. However, as the cell sizes are aggressively shrunk to the nanoscale regime, they are adversely affected by the discrete nature of Q_T . Thus, we must consider all possible tunneling paths across the defective oxide [35][36], as schematically shown in **Figure 2** b, which increases the computational time and complexity of the method.

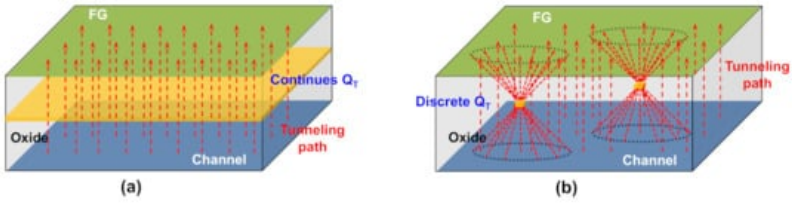

Figure 2. Schematic diagrams of all the possible tunneling paths by the (**a**) continuous and (**b**) discrete QT during P/E cycles.

The second category of methods is based on the direct extraction of Q_T and Q_{FG} using a special test device [37][38]. The cross-sectional view and equivalent circuit of the test structure are shown in **Figure 3** . The device is composed of two memory cells: one with a thick tunneling oxide, referred to as a high-voltage (HV) cell, and the other with a thin tunneling oxide, referred to as a low-voltage (LV) cell. Notably, these two cells have a common FG/common control gate (CG) configuration. During P/E operations, FN tunneling occurs only through the oxide of the LV cell, thus degrading the oxide of this cell. The ES resulting from Q_T is expressed as [38]:

$$\mathrm{ES} = \gamma[\Delta V_T(LV) - \Delta V_T(HV)] = -\frac{1}{\varepsilon_{ox}} \int_0^{T_{OX}} \rho \cdot x dx \quad (2)$$

(2)

where γ is the coupling ratio between the FG and CG, ρ is the density of Q_T , and $\Delta V_T(LV)$ and $\Delta V_T(HV)$ are the V_T shifts of the LV and HV cells after P/E cycles, respectively. Unfortunately, the size of the test device (L = 4 μm) is relatively large compared to that of conventional NAND Flash memories, yet it is necessary to continuously evaluate these miniaturized and new device structures. Moreover, this approach can only provide average information for a relatively large sample region rather than statistical information.

3. ΔGm, max Statistics

Experiments are carried out in 2D FG-type NAND Flash memory chip. In the NAND array, a string is composed of 32-unit cells, a source-select transistor, and a drain-select transistor, as schematically shown in **Figure 4** a. The control gates, source-select transistors, and drain-select transistors are connected across different strings to constitute the wordline (WL), source select line (SSL), and drain select (DSL), respectively. The strings are connected to a common sourceline (SL) and bitlines (BLs). The channel length (L) and width (W) are both 42 mm, and the tunneling oxide thickness (T_{ox}) is 8 nm. The measurement scheme was as follows: the program operation is performed by adopting the incremental step pulse programming (ISPP) technique [39] with a starting CG voltage ($V_{CG,0}$,0) in increments of 0.2 V with a duration of 10 µs, as schematically shown in **Figure 4** b, driving the selected cells to the desired V_T level. The erase operation is performed on blocks by adopting the incremental step pulse erasing (ISPE; similar to the ISPP) technique. Because it is not possible to apply high negative voltages in NAND chips, a high positive voltage is applied to the p-well. As a result, all cells in the block were erased simultaneously. During the read operation, the CG gate voltage was swept from 0 V to 5 V to harvest the maximum transconductance reduction ($\Delta G_{m,max}$). **Figure 5** a shows the $I_D - V_{CG}$ characteristics of the 200 randomly selected cells on WL15 in NAND strings before cycling and after 1 k, 3 k, and 30 k P/E cycles, respectively. Then, the corresponding $\Delta G_{m,max}$ distribution can be obtained, as shown in **Figure 5** b. Notably, the endurance test and Δ G m ,m a x monitoring were performed at room temperature. The mean value of $\Delta G_{m,max}$ ($\overline{\Delta G}_{m,max}$) is clearly observed to increase, and the distribution to become wider, as the number of cycles increases. This suggests that the $\Delta G_{m,max}$ distribution will be a good parameter for evaluating the oxide degradation.

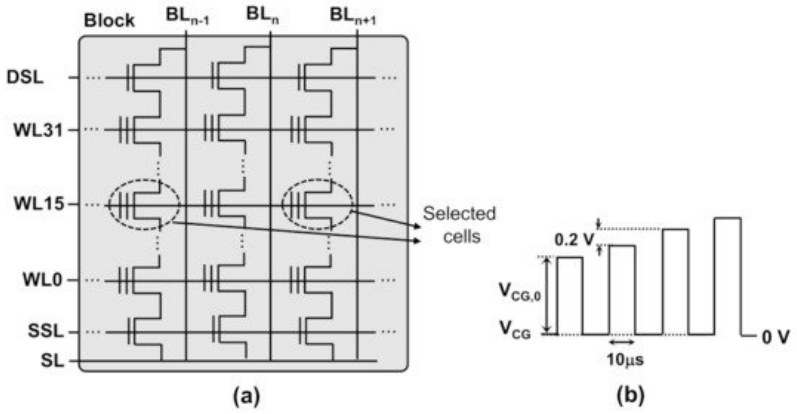

Figure 4. Schematic view of (**a**) NAND Flash array and (**b**) ISPP operation. Adapted from [40].

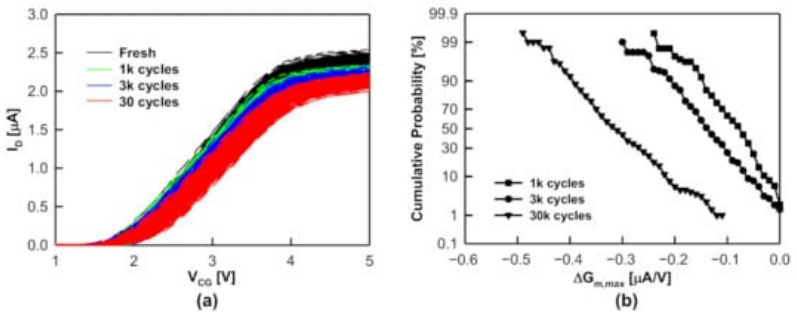

Figure 5. (**a**) $I_D - V_{CG}$ Characteristics and (**b**) cumulative ΔGm,max statistics of the read cells on WL15 as a function of the number of P/E cycles. Adapted from [39].

Monte Carlo simulations have been used in an attempt to extract information about Q_T from the measured Δ G m ,m a x distribution. A NAND string can be modeled to have a selected cell with equivalent source and drain resistances (R_S and R_D), as shown in **Figure 6** a. The equivalent (R_S and R_D can be extracted from the monitoring of the transconductance of the read cells for different positions along the NAND string [41]. The equivalent R_S and R_D are 130 kΩ and 138.2 kΩ, respectively. The TCAD simulations used a 3D drift-diffusion equation and coupled with the Shockley–Read– Hall model for generation/recombination and mobility models (including the electric field dependence, doping-dependent modification, and surface mobility degradation). To determine the $\overline{\Delta G}_{m,max}$ statistics accurately, the simulated $I_D - V_{CG}$ characteristic of the fresh cell is calibrated with experimental data at a probability level p = 50% , as shown in **Figure 6** b. The simulation was in good agreement with the experimental results. After calibrating the equivalent resistances, the Monte-Carlo-based method was adopted to evaluate the concentration of Q_T (Q_T^C) after P/E cycles, as schematically shown in **Figure 7** . The step-by-step procedure is as follows: First, discrete Q_T is randomly generated

following a uniform distribution in a cuboid volume 420 nm × 840 nm × 8 nm in size (i.e., 20 L × 10 W × T o x), with an equivalent Q_T^C . Notably, the discrete Q_T is treated as a negative point charge corresponding to one electron because the electron mobility is degraded by the Coulomb repulsion.

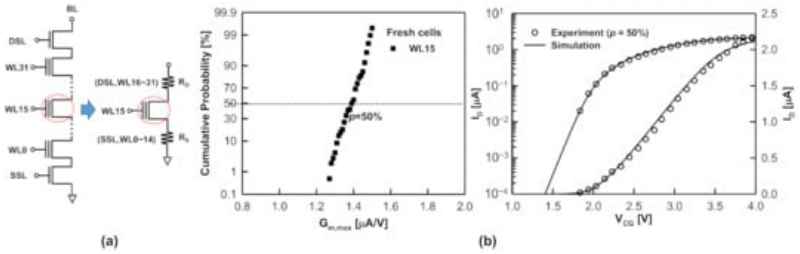

Figure 6. (**a**) Schematic circuit diagram of a NAND string and an equivalent model when cells on WL15 are read. (**b**) Comparison between measured and simulated $I_D - V_{CG}$ curve of cells on WL15 at ***p*=50%**, plotted on the linear and logarithmic scales. Adapted from [39].

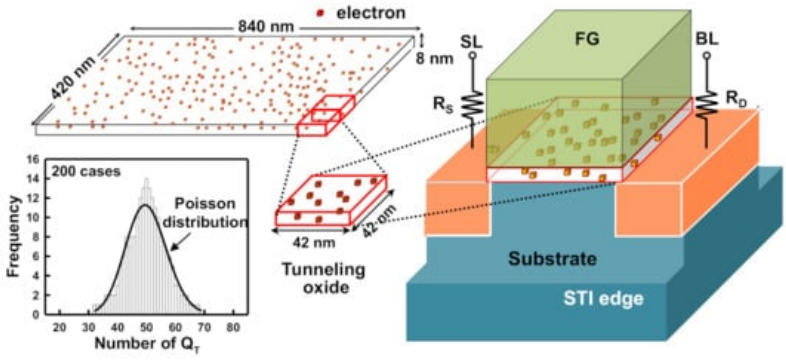

Figure 7. Schematic diagram of the random discrete Q_T generating algorithm. Adapted from [39].

Second, the cuboid is partitioned into 200 sub-cuboids and then mapped into the tunneling oxide region. Thus, the numbers of discrete Q_T in these 200 cases approximately follow a Poisson distribution, as shown in **Figure 7** . Finally, a comparison of the simulated and measured Δ G m ,m a x statistics allowed us to evaluate the Q_T^C during P/E cycles.

Moreover, even though the simulation does not directly account for interface trap (D_{it}) generation, the effect thereof is reflected in the model. The measured $I_D - V_{CG}$ characteristics indicated that the transconductance reached a maximum when V_{CG} slightly exceeded D_{it} ; therefore, the occupied D_{it} can be considered as a fixed Q_T located at the silicon/oxide interface because the bending of the surface potential remains almost unchanged [42] (see **Figure 8**).

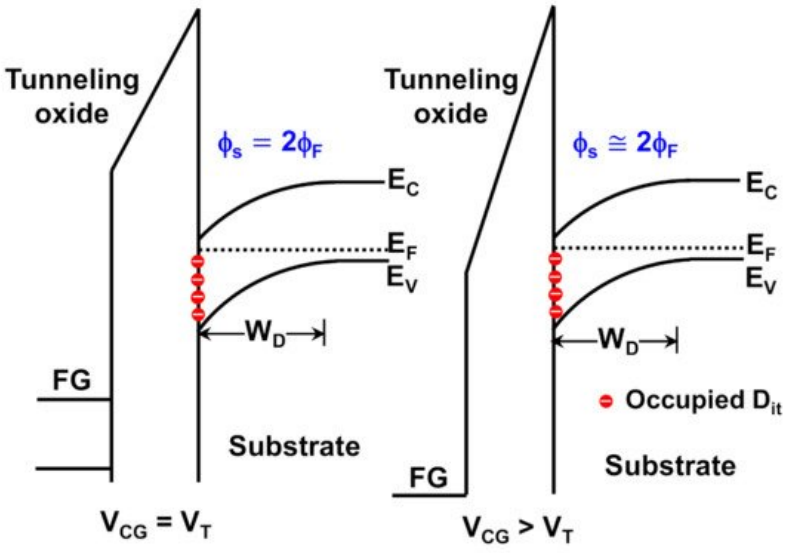

Figure 8. Band diagram and trap occupation of interface trap states at different biases. Reprinted from [39].

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