Single-Phase Fault Tolerant Multilevel Inverters Topologies

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Multilevel inverters (MLIs) are used in a variety of industrial applications in high- and medium-voltage systems. The modularity, high-power output from medium voltages, and low harmonic content are some of the advantages of MLIs. The reliability of MLIs is quite important. The reliability is affected by different kinds of faults occurring in the MLIs. In MLI circuits, switching devices are the most vulnerable components and have a major involvement in all types of faults. As an outcome, it is necessary to take proper corrective action in the event of a fault.

fault tolerant | fault-tolerant multilevel inverter | reduced device count

1. Introduction

Multilevel inverters are gaining importance in medium-voltage and high-power industrial applications [1][2]. The three MLI topologies, i.e., cascaded H-bridge (CHB), neutral point clamped (NPC), and flying capacitor (FC), are included in classical MLI topologies [3][4]. MLIs find applications in standalone or grid-connected PV systems [5][6][7][8], pumped storage power plants [9], active power filters [10][11], flexible AC transmission systems (FACTSs) [12], variable frequency drives [13], high-voltage DC (HVDC) system [14][15], etc.

2. Single-Phase FT MLIs

2.1. TP1 and TP2

Other authors modified a cross-connected-sources-based MLI (CCS-MLI) and T-type MLI for FT operation in [16] by connecting switches S_1 and S_2, respectively. Both MLIs are single-phase five-level inverters. A phase opposition disposition sinusoidal PWM (POD-SPWM) scheme is employed for generating switching pulses in both the topologies. Both the topologies use the SA FT solution for fault tolerance.

The topology TP1, i.e., modified CCS-MLI, comprises two DC sources, one bidirectional switch (S_1), and six unidirectional switches. It can generate only three levels for a single-switch OC fault in faulty conditions. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A lower number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

The topology TP2, i.e., modified T-type inverter, comprises two DC sources, two bidirectional switches (T_1 and S_2), and four unidirectional switches. It can generate three or five levels for a single-switch OC fault in faulty conditions. The topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A lower number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

2.2. TP3 and TP4

Other authors modified a single-phase five-level Packed U-Cell MLI (PUC-MLI) and single-phase seven-level symmetrical and asymmetrical MLI topology for FT operation in [17] by connecting switches S_1 and S_2, and R_1 and R_2, respectively. A level-shifted SPWM (LS-SPWM) scheme is employed for generating switching pulses in both topologies. Both topologies use the SA FT solution for fault tolerance.

The topology TP3, i.e., modified PUC MLI, comprises one DC source, one capacitor, and eight unidirectional switches. It can generate three or five levels for a single-switch OC fault in a faulty condition. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A smaller number of switches is the merit of the topology. The limitations of topology are the inability to tolerate multiple-switch faults and decreased output voltage levels under post-fault conditions.

The topology TP4, i.e., modified symmetrical and asymmetrical MLI, comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. Switches (S_1, R_1, and R_2) are bidirectional switches. It can generate five levels for a single-switch OC fault in a faulty condition. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A smaller number of switches is the merit of the topology. The limitations of topology are the use of bidirectional switches, the inability to tolerate multiple-switch faults, and decreased output voltage levels under post-fault conditions.

2.3. TP5

A single-phase five-level FT MLI topology (TP5) is proposed in [18]. The authors added a redundant leg to the full-bridge NPC inverter topology to make it FT. TP5 has a main inverter and a redundant leg. TP5 comprises two DC sources, four diodes, four fuses, and fourteen unidirectional switches. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the LA FT solution for fault tolerance. This topology is able to generate voltage levels by using the same or a smaller number of switching devices (IGBTs). The efficiency achieved in the post-fault condition is the same or even higher than in the pre-fault condition. The topology tolerates SC faults by using fewer fuses compared to other topologies. The topology can handle single and multiple OC and SC switch faults in one or two legs of the main inverter circuit. The merits of the topology include no use of bidirectional switches, fewer conducting switches in post-fault conditions, and the preservation of all output voltage levels for all single and multiple (two switches) switch faults. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology.

2.4. TP6

Another single-phase five-level FT MLI topology (TP6) is proposed in [3]. The authors combined a conventional flying capacitor (FC) leg, cascaded H-bridge (CHB) leg, and active neutral point clamped (ANPC) leg to develop FT topology. TP6 has a main inverter and a redundant leg. It comprises one DC source, one capacitor, and twelve unidirectional switches. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. The topology has the ability to tolerate single- and multiple-switch OC faults in the circuit. The merits of topology include no use of bidirectional switches, the efficiency achieved in post-fault conditions being the same as the healthy operation, preservation of the output power in the faulty condition same as in the healthy operation, and self-balancing of flying capacitor voltage. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology. The topology was used in [19] for more electric aircraft applications.

2.5. TP7

A single-phase nine-level FT MLI topology (TP7) is proposed in [20]. The FT MLI consists of the main inverter and the redundant leg. The main inverter is composed of two three-level flying capacitor legs. TP7 comprises two DC sources, two capacitors, and sixteen unidirectional switches.

The phase-disposition SPWM (PD-SPWM) scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. The topology does not include any bidirectional switches. The topology can generate voltage levels under single and multiple OC faults while preserving output power both in healthy and post-fault operations. The merits of this topology include the efficiency achieved in post-fault conditions being higher as compared with the healthy operation, the ability to tolerate single- and multiple-switch OC and SC faults, and the self-balancing of the flying capacitor voltage both in healthy and post-fault operation. No utilization of redundant legs' switches under healthy conditions is the limitation of the topology.

2.6. TP8 and TP9

A single-phase five-level FT MLI topology is proposed in [21]. Two topologies are proposed in the publication. In the first topology (TP8), there is a loss of levels in output voltage after a fault; this is termed partial fault tolerance. In the second topology (TP9), there is no loss of levels in output voltage after a fault; this is termed complete fault tolerance. The LS-SPWM scheme is employed for generating switching pulses in both topologies. TP8 and TP9 use IHR and LA FT solutions, respectively, for fault tolerance.

The first part of the publication discusses the partial solution to the faults since there are losses of levels. TP8 comprises one DC source, one capacitor, two diodes, one bidirectional switch, and six unidirectional switches. This partial solution topology can be generalized for any number of levels by cascading basic topology. The topology achieves the self-balancing of the capacitor voltage both in healthy and faulty operation. The capacitor voltage ripples increase under post-fault operation. This topology can tolerate all single-switch OC and SC faults in the circuit with loss of levels. The merits of the topology include the self-balancing of the capacitor voltage under faulty conditions, 100% utilization of all switches under healthy conditions, and FT MLI can be extended by cascading

similar units depending upon the number of output voltage levels needed. The use of bidirectional switches, the inability to preserve all output voltage levels for all single-switch faults, the increase in capacitor voltage ripples under post-fault operating conditions, and the inability to tolerate multiple-switch faults are the limitations of the topology.

The second part of the publication discusses the complete solution to the faults since there is no loss of levels. TP9 has a main inverter and a redundant leg. It consists of one DC source, one capacitor, two diodes, three bidirectional switches, and eight unidirectional switches. The topology TP9 achieves the self-balancing of the capacitor voltage both in healthy and faulty operation. The capacitor voltage ripples under post-fault operation remain the same as in pre-fault operation. The topology can tolerate all single-switch OC and SC faults in the circuit without loss of levels. The redundant legs' switches are only utilized in the case of a fault. The merits of the topology include the self-balancing of the capacitor voltage under faulty conditions, no increase in capacitor voltage ripples under post-fault operating conditions, and the preservation of all output voltage levels for all single-switch faults. The use of bidirectional switches, higher cost, no utilization of redundant legs' switches under healthy conditions, higher number of conducting switches under post-fault condition (hence it results in higher switching power loss under post-fault condition), and inability to tolerate multiple-switch faults are the limitations of the topology.

2.7. TP10

An FT MLI topology (TP10) presented in [22] by modifying the FT MLI topology given in [21]. The authors added a novel redundant leg to the main inverter. TP10 consists of one DC source, one capacitor, two diodes, one bidirectional switch, and twelve unidirectional switches. The circuit of topology**.**

The LS-SPWM scheme is employed for generating switching pulses in the topology. TP10 uses the LA FT solution for fault tolerance. The main inverter has a drawback of lesser post-fault efficiency as compared to pre-fault efficiency. This limitation is solved by proposing a novel redundant leg. The novel redundant leg provides an overload-current-sharing characteristic, which is absent in the original topology. It is capable of working at reduced voltage levels if a switch fault occurs. It can tolerate single-switch OC faults with preserved power. Overload-current-handling capability by utilizing redundant legs' switches under healthy conditions is the merit of the topology. The limitations of the topology include a higher number of conducting switches under post-fault conditions (hence, it results in higher switching power loss under post-fault conditions).

2.8. TP11

A single-phase five-level FT MLI topology (TP11) is proposed in [23]. The topology TP11 is capable of tolerating OC and SC faults for single and multiple switches. TP11 comprises one DC source, one capacitor, two diodes, four fuses, and twelve unidirectional switches. It consists of a main inverter and a redundant leg. The main inverter topology is constructed by using the legs of conventional three-level neutral point clamped inverter and three-level flying capacitor inverter. The redundant leg is constructed by using a conventional three-level cascaded H-bridge

(CHB) inverter. The LS-SPWM scheme is employed for generating switching pulses in the topology. TP11 uses the LA FT solution for fault tolerance. The main feature of the topology is to tolerate single- and multiple-switch faults, no matter whether they are OC or SC faults. The merits of the topology include inherent capacitor voltage balancing under both single-switch and multiple-switch faults; multiple-switch faults tolerance for any pair, triplet, or quadruple of switches; and output power will remain to preserve post-fault, similar to pre-fault output power. Decreased voltage levels (leading to higher harmonic distortions of the output voltage waveform) and no utilization of redundant legs' switches under healthy operation are the limitations of the topology.

2.9. TP12

A single-phase five-level FT MLI (TP12) is proposed in [24]. The authors named it DITHB, i.e., developed inverter with two half-bridges. TP12 comprises two DC sources and nine unidirectional switches. The LS-SPWM scheme is employed for generating switching pulses in the topology. TP12 uses the IHR FT solution for fault tolerance. In faulty conditions, the topology can generate three levels for a single-switch OC fault. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. A higher number of conducting switches under healthy and faulty conditions is the limitation of the topology. The following are the merits of the topology:

- It has switching states which can bring two sources in parallel. Due to this advantage, it is possible to maintain power in post-fault similar to the pre-fault power.
- Single unit can be connected in series depending upon the number of output voltage levels required.

2.10. TP13

A single-phase thirteen-level FT MLI (TP13) is proposed in [25]. TP13 comprises three DC sources, three bidirectional switches, and six unidirectional switches. The nearest level control PWM (NLC-PWM) scheme is employed for generating switching pulses in the topology. TP13 uses the SA FT solution for fault tolerance. This topology can tolerate a single-switch OC fault in the circuit with a loss of levels. The merit of the topology includes the ability to tolerate all single-switch OC faults. The limitations of the topology include a higher number of bidirectional switches and the inability to tolerate multiple-switch faults.

2.11. TP14

The authors of another study modified a single-phase nine-level cascaded H-bridge (CHB) inverter with an asymmetrical configuration for fault tolerance in [26]. TP14 comprises two DC sources and ten unidirectional switches. A hybrid modulation technique comprising NLC and LS-PWM is employed for generating switching pulses in the topology. TP14 uses the SA FT solution for fault tolerance. It can tolerate switch OC faults. It utilizes two redundant switches, R_1 and R_2, to provide fault tolerance under faulty conditions. The merit of the topology includes the ability to tolerate all single-switch OC faults. The inability to tolerate all multiple-switch OC and SC faults is the limitation of the topology.

2.12. TP15 and TP16

A generalized single-phase FT MLI is proposed in [27]. It can work in symmetric and asymmetric modes. When all the sources are equal, the mode of operation is called symmetric, whereas when sources are different, the mode of operation is called asymmetric. TP15 and TP16 comprise four DC sources and twelve unidirectional switches. The modified level-shifted carrier PWM (LSCPWM) scheme is used for generating the gating pulses in the topology. Both topologies use the IHR FT solution for fault tolerance. The proposed topology can tolerate single- and multiple-switch OC and SC faults. The proposed topology can operate under both symmetric and asymmetric modes. The proposed topology can generate higher voltage levels with respect to its modular structure. The switches R_{1a} and R_{a2} operate only in the case of switch R_1 and R_2 failure. The ability to tolerate both source and/or switches faults and the ability to extend topology depending upon the number of output voltage levels requirement are the merits of the topology. No utilization of switches R_{1a} and R_{a2} under healthy operation is the limitation of the topology.

2.13. TP17

A single-phase five-level FT MLI (TP17) is proposed in [8]. TP17 comprises two DC sources, two diodes, one bidirectional switch, and six unidirectional switches. The phase-disposition sinusoidal PWM (PD-SPWM) scheme is employed for generating switching pulses in the topology. The topology uses the SA FT solution for fault tolerance. If a fault occurs in the source and/or switch, the topology can generate three voltage levels instead of five levels. The output voltage magnitude reduces after the fault. Therefore, to maintain the rated output voltage, a transformer is used. The merits of the topology are as follows:

- TP17 topology is capable of tolerating faults caused by the failure of the source.
- TP17 reduces the uneven charging of batteries that is caused to partial shading or hotspots on one side of the PV panels due to energy-balancing between sources.

The limitations of the topology are as follows:

- Use of bidirectional switch.
- Inner leg switches in the NPC leg are not FT.
- Implementation of center-tapped transformer.

2.14. TP18

A single-phase nine-level FT MLI topology (TP18) is proposed in [28]. TP18 comprises two DC sources, one capacitor, three bidirectional switches, and six unidirectional switches.

The PD-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can generate nine levels, using three bidirectional and six unidirectional switches and a capacitor under healthy operation. It does not need any redundant leg or extra switches. It is capable of working at reduced voltage levels if a switch fault occurs. The merits of the topology include 100% utilization of all switches in healthy condition, and the switching scheme proposed in the work achieves the natural capacitor voltage balancing without any external circuit. The use of a higher number of bidirectional switches is the limitation of the topology.

2.15. TP19

A single-phase five-level FT MLI (TP19) is proposed in [29]. The proposed inverter topology is capable of tolerating both OC and SC faults on all single switches and some multiple switches. TP19 comprises two DC sources, nine fuses, three bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. The switches A_6 and A_7 operate only under FT operation. A fast-acting switch is used in series with each switch to detect SC faults. The controller sees a short circuit as an open circuit and provides separate operations for OC and SC faults. The merits of the topology include the ability to tolerate both OC and SC faults and the ability to provide rated output voltage and power under any switch fault. The use of a higher number of bidirectional switches and no utilization of switches A_6 and A_7 under healthy conditions are the limitations of the topology.

2.16. TP20

A single-phase nine-level FT MLI topology (TP20) is proposed in [30]. TP20 comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for generating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology is unable to provide rated output voltage and power in some faults. A smaller number of conducting switches under post-fault conditions is the merit of the topology. The use of a higher number of bidirectional switches and the inability to tolerate fault on the bidirectional switch connected between the capacitor and load terminal are the limitations of the topology [20][31].

2.17. TP21

A single-phase eleven-level FT MLI topology (TP21) is proposed in [32]. TP21 comprises three DC sources, three bidirectional switches, and six unidirectional switches. The publication deals only with OC faults. The switches A_8 and A_9 work only under faulty conditions. The NLC-PWM scheme is employed for generating switching pulses in the topology. The topology uses the SA FT solution for fault tolerance. The ability to tolerate all single-switch OC faults and some multiple-switch OC faults is the merit of the topology. The use of bidirectional switches, no utilization of switches A_8 and A_9 under healthy conditions, and the inability to tolerate SC faults are the limitation of the topology.

2.18. TP22

A fifteen-level FT MLI topology (TP22) is proposed in [33], TP22 comprises four DC sources, one bidirectional switch, and ten unidirectional switches. This FT MLI topology does not utilize additional hardware components to create redundancy for FT operation. It utilizes inherent hardware redundancy for fault tolerance. It is able to tolerate all single-switch OC faults. A combination of nearest level modulation (NLM) and selective harmonic elimination (SHE) is employed for generating switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The merit of the topology includes 100% utilization of all switches under healthy conditions. The use of a higher number of DC sources is the limitation of the topology.

2.19. TP23

Other authors proposed a five-level FT MLI topology (TP23) in [34] by modifying a five-level modified PUC (MPUC5) inverter topology. Three redundant switches (A_7, A_8, and A_9) are added to the original MPUC5. TP23 comprises two DC sources and nine unidirectional switches. This topology can tolerate all single-switch OC faults. The NLC-PWM scheme is used for generating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. The use of a smaller number of switches is the merit of the topology. The limitations of the topology include the inability to tolerate SC faults and multiple-switch faults.

2.20. TP24 and TP25

The authors in [35] proposed FT MLI topologies (TP24 and TP25). Topologies TP24 and TP25 comprise four DC sources and twelve unidirectional switches. Two switches, A_{7r} and A_{8r}, are used as redundant switches. It can generate 9 levels and 17 levels of waveform depending upon the values of DC sources. The topology TP24 generates nine levels with $V_{dc1} = V_{dc2} = V_{dc3} = V_{dc4} = V$ in the symmetric mode of operation. The topology TP25 generates 17 levels with $V_{dc1} = V_{dc2} = V$, and $V_{dc3} = V_{dc4} = 3V$ in the asymmetric mode of operation. It can tolerate all single- and multiple-switch OC faults. The modified LSCPWM scheme is used for generating the gating pulses in the topology. TP24 and TP25 use the IHR FT solution for fault tolerance. The merit of the topology includes its lower total standing voltage (*TSV*). The inability to tolerate the SC fault on all switches is the limitation of the topology.

2.21. TP26

A single-phase five-level FT MLI is proposed in [36]. It comprises two DC sources, two bidirectional switches, and four unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can tolerate OC single-switch faults in all switches and some OC double-switch faults. The topology can be generalized for the “N” number of levels. This FT MLI topology can be used in solar-based charging station applications. The topology is used in [37] for wave power plant applications. The merit of the topology includes 100% utilization of all switches under healthy conditions. The use of bidirectional switches is the limitation of the topology.

2.22. TP27 and TP28

A single-phase seven-level FT MLI is proposed in [38]. It comprises three DC sources, five bidirectional switches, and five unidirectional switches. The topology is modular in nature. It can be generalized for the “N” number of levels. The seven-level FT MLI can be modified and made into a nine-level FT MLI by adding a module consisting of one DC source, one bidirectional switch, and one unidirectional source. The POD-SPWM scheme is used for creating the gating pulses in the topology. TP28 uses the IHR FT solution for fault tolerance. The topology can tolerate OC single- and double-switch faults in switches and OC and SC faults in sources. The modular nature and ability to extend the topology for the “N” number of output voltage levels are the benefits of this topology.

2.23. TP29

A single-phase FT MLI is proposed in [39] for multi-string photovoltaic (PV) applications. It consists of two H-bridges and comprises four DC sources, two bidirectional switches, and ten unidirectional switches. This topology can synthesize a nine-level output voltage under symmetric conditions ($V_1 = V_2 = V_3 = V_4 = V/4$). This topology can synthesize a thirteen-level output voltage under asymmetric conditions ($V_1 = V_2 = V/6$ and $V_3 = V_4 = V/3$). The PD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. In the event of partial shading of PV panels, TP29 is capable of energy balancing between sources.

2.24. TP30

A single-phase seven-level FT MLI is proposed in [40]. It comprises three DC sources, two bidirectional switches, and eight unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to the “N” number of output voltage levels. It can tolerate single-switch OC faults on switches.

2.25. TP31

A single-phase nine-level FT MLI is proposed in [41]. It comprises four DC sources, three bidirectional switches, and six unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. It can tolerate single- and multiple-switch OC faults.

2.26. TP32

A single-phase five-level FT MLI is proposed in [42]. It comprises two DC sources, two bidirectional switches, and four unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to the “N” number of output voltage levels. TP32 can tolerate OC/SC faults in sources. It can also tolerate all single OC faults and some multiple OC faults in switches.

2.27. TP33

A single-phase FT MLI is proposed in [43]. It comprises three DC sources, four bidirectional switches, and four unidirectional switches. This topology can synthesize a seven-level output voltage under symmetric conditions (same DC sources) and term it TP33A. This topology can synthesize a thirteen-level output voltage under asymmetric conditions (different DC sources) and term it TP33B. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. The topology can be extended to the “N” number of output voltage levels. TP33 can tolerate OC faults in all switches. A higher number of bidirectional switches is the limitation of this topology.

2.28. TP34

A single-phase seven-level FT MLI is proposed in [44]. It comprises three DC sources and eight unidirectional switches. A sine wave reference with an inverted sine carrier pulse generation scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. It can tolerate all single-switch OC faults.

2.29. TP35

A single-phase five-level FT MLI is proposed in [45]. It comprises a single DC source, two capacitors, two bidirectional switches, and four unidirectional switches. The POD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP35 can tolerate all single-switch OC faults. It can also tolerate any OC fault occurring in any leg of the H-bridge. This topology also achieves the self-balancing of the DC-link capacitors.

2.30. TP36

A single-phase seven-level FT MLI is proposed in [46]. It comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. TP36 can tolerate all single-switch OC faults. This topology also achieves the self-balancing of the DC-link capacitors.

2.31. TP37

A single-phase fifteen-level FT MLI is proposed in [47]. It comprises a single DC source, eight capacitors, six bidirectional switches, and twenty-four unidirectional switches. The NLM-PWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP37 can boost the input voltage seven times according to the concept of a switch capacitor. This topology can tolerate both OC and SC faults on single and multiple switches. This topology also achieves the self-balancing of the DC-link capacitors. The requirement of a single DC source is the merit of the topology.

2.32. TP38

A single-phase nine-level FT MLI is proposed in [48]. It comprises four DC sources, two bidirectional switches, and eight unidirectional switches. POD-SPWM and NLC-PWM schemes are used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP38 can tolerate all single-switch OC faults. The requirement of a higher number of DC sources is the limitation of the topology.

2.33. TP39

A single-phase nine-level FT MLI is proposed in [49]. It comprises two DC sources, two capacitors, four bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the SA FT solution for fault tolerance. TP39 achieves self-voltage balancing of DC-link capacitors under healthy and faulty conditions. The topology can tolerate both single-switch and multiple-switch faults. The use of a higher number of bidirectional switches is the limitation of the topology.

2.34. TP40

A single-phase five-level FT MLI topology is proposed in [50]. The authors added a redundant leg to the conventional five-level NPC inverter to make it FT. The topology has a main inverter and a redundant leg. It comprises a single DC source, six diodes, two capacitors, and fourteen unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP40 can tolerate both single-switch and multiple-switch OC and SC faults.

2.35. TP41

A single-phase seven-level FT MLI is proposed in [51]. It comprises three DC sources, six relays, two bidirectional switches, and four unidirectional switches. The NLC-PWM technique is employed for generating the switching pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP41 can tolerate all single-switch OC faults.

2.36. TP42

A single-phase five-level FT MLI is proposed in [52]. It comprises two DC sources, one bidirectional switch, and six unidirectional switches. The LS-PWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP42 can tolerate all single-switch OC faults.

2.37. TP43

A single-phase nine-level FT MLI topology is proposed in [53]. The topology has a main inverter and a redundant leg. It comprises two DC sources, two capacitors, three bidirectional switches, and six unidirectional switches. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP43 can tolerate all single-switch OC faults.

2.38. TP44

A single-phase five-level FT MLI is proposed in [54]. It comprises two DC sources, two relays, one bidirectional switch, and four unidirectional switches. Using relays, it is possible to bypass faulty switches and create symmetrical output voltages under faulty conditions. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance. TP44 can tolerate all single-switch OC faults.

2.39. TP45

A single-phase nine-level FT MLI is proposed in [55]. TP45 is the modified form of the topology that is proposed in [56]. It comprises two DC sources, two capacitors, and thirteen unidirectional switches. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the IHR FT solution for fault tolerance.

2.40. TP46

A single-phase nine-level FT MLI topology is proposed in [57] for PV applications. The topology has the main inverter and the redundant leg. It comprises three DC sources, seven fuses, three bidirectional switches, and six unidirectional switches. A fast-acting fuse is connected to each switch in the main inverter. The LS-SPWM scheme is employed for generating switching pulses in the topology. The topology uses the LA FT solution for fault tolerance. TP46 can tolerate single- and multiple-switch OC and SC faults.

3. Single-Phase FT MLIs Based on Module

3.1. TP47 and TP48

The authors of another study modified the CHB MLI and provided fault tolerance through their proposed scheme in [58]. The circuit of the single-phase seven-level FT MLI (TP47) (symmetric CHB, i.e.,. The circuit of the single-phase fifteen-level FT MLI (TP48) (asymmetric CHB, i.e.,. This MLI topology consists of three CHB cells connected in cascade and one load-side H-bridge cell. The fault is removed by two relays. Each cell has one normally open (NO) and one normally closed (NC) conductor of each relay. The load-side H-bridge cell has two normally open (NO) and two normally closed (NC) conductors of each relay. The authors proposed an FT scheme for this MLI. The cascaded full-bridge CHB cells reconfigure to cascaded half-bridge CHB cells when the first fault occurs. The cascaded half-bridge CHB cells reconfigure to series-connected dc sources when a second fault occurs. This is the basic principle of this FT scheme. TP47 and TP48 use MB FT solution for fault tolerance.

The merits of the topology include the use of a smaller number of relays, low voltage stress exerted on healthy switches in case of fault, and utilization of all dc voltage sources under post-fault conditions. The limitations of the topology are as follows:

- Load side CHB cannot be made FT with fewer devices [3].
- Cannot generate pre-fault power after multiple-switch faults [20].

3.2. TP49

An FT structure and control scheme for CHB MLI are presented in [59]. Each CHB module has four relays. The topology uses MB FT solution for fault tolerance. In any module's switch fault (OC or SC fault), the proposed control scheme eliminates the defected module from the circuit. The MLI continues the power supply with reduced voltage levels, with the remaining healthy modules. The merit of the topology includes the ability to tolerate both OC and SC switch faults. The limitations of the topology are as follows:

- High voltage stress is exerted on healthy switches in case of fault [58].
- Higher conduction losses.
- Higher cost.

3.3. TP50 and TP51

Other authors proposed a three-phase hybrid CHB FT MLI by adding an X-CHB inverter to the CHB inverter in [60]. The proposed three-phase inverter can generate an "N" number of levels. TP50 and TP51 use MB FT solution for fault tolerance. If a switch fault occurs in any H-bridge cell, the faulty H-bridge cell is bypassed and provides power from the remaining H-bridge cells and X-CHB cell. The proposed topology continues to deliver power at pre-fault voltage levels in case of OC or SC switch faults. It also provides self-balancing capacitor voltage. Battery energy storage systems (BESSs) and uninterrupted power systems are good examples of industrial applications that can utilize the topology. The merits of the topology include the ability to tolerate OC or SC faults and the ability to extend topology to an "N" number of levels. A higher device count is the limitation of the topology.

3.4. TP52

A single-phase thirteen-level FT MLI is proposed in [61]. The topology consists of three modified CHB bridge modules. Each module comprises two DC sources and six unidirectional switches. One module always acts as a redundant module. Overall, the topology comprises six DC sources and eighteen unidirectional switches. The thirteen-level output is synthesized by two modules, whereas the faulty module is bypassed. The LS-SPWM scheme is used for creating the gating pulses in the topology. The topology uses the MB FT solution for fault tolerance. All the modules are equally used during normal operation. TP52 can tolerate single-switch OC and SC faults.

3.5. TP53

A single-phase seven-level FT MLI is proposed in [62]. It comprises three DC sources, sixteen relays, and twelve unidirectional switches. During faulty operation, relays are used to reroute conducting paths. It is important to note that T_{S1} to T_{S7} are single-pole, single-throw (SP-ST) relays, and T_{D1} to T_{D9} are single-pole, double-throw (SP-DT) relays [62]. The PD-SPWM scheme is used for creating the gating pulses in the topology. The topology uses MB FT

solution for fault tolerance. When one module is faulty, the faulty module is isolated, and the faulty module's source is connected in series with one of the sources of healthy modules. If one module becomes faulty, the TP53 can continue to provide the same output voltage waveform and amplitude, as it did in the pre-fault operation. The use of a large number of relays is the drawback of this topology.

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