Barrier Layer of Cu Interconnects

Subjects: Chemistry, Physical
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The barrier layer in Cu technology is essential to prevent Cu from diffusing into the dielectric layer at high temperatures; therefore, it must have a high stability and good adhesion to both Cu and the dielectric layer. In the past three decades, tantalum/tantalum nitride (Ta/TaN) has been widely used as an inter-layer to separate the dielectric layer and the Cu. However, to fulfill the demand for continuous down-scaling of the Cu technology node, traditional materials and technical processes are being challenged. Direct electrochemical deposition of Cu on top of Ta/TaN is not realistic, due to its high resistivity. Therefore, pre-deposition of a Cu seed layer by physical vapor deposition (PVD) or chemical vapor deposition (CVD) is necessary, but the non-uniformity of the Cu seed layer has a devastating effect on the defect-free fill of modern sub-20 or even sub-10 nm Cu technology nodes. New Cu diffusion barrier materials having ultra-thin size, high resistivity and stability are needed for the successful super-fill of trenches at the nanometer scale. In this review, we briefly summarize recent advances in the development of Cu diffusion-proof materials, including metals, metal alloys, self-assembled molecular layers (SAMs), two-dimensional (2D) materials and high-entropy alloys (HEAs). Also, challenges are highlighted and future research directions are suggested.

Cu diffusion barrier | platinum group metals | 2D materials | self-assembled monolayers

1. Introduction

Ever since the development of the integrated circuit (IC) about 60 years ago, aluminum (Al) and silicon dioxide (SiO_2) have been most widely used as conductor and insulator materials for the fabrication of micro-processors [1][2]. As technical demands grew, the continuous decrease of the feature sizes and the explosive increase of the number of transistors in micro-processors resulted in the growth of so-called gate delays [3][4]. To solve this issue, new wiring materials with resistivity lower than Al and dielectric materials with dielectric constant (so-called low-κ) lower than conventional SiO_2 have to be used as alternatives. IBM announced in 1997 the replacement of Al with copper (Cu) as the interconnect material in semiconductor processing [5]. As compared to Al, Cu has a smaller gate delay due to its lower electrical resistivity, but higher electro-migration, stress-migration resistances and melting point [6]. However, a big problem of switching Al to Cu is that the conventional methods used for Al deposition (sputter deposition) and patterning (reactive ion etching) are not suitable for Cu, as Cu is corroded during standard chip manufacturing processes. Therefore, the fabrication technique has to be upgraded for Cu patterning and deposition.

The structure of Cu interconnects is usually patterned by a so-called damascene process [7][8], in which the dielectric layer is patterned in advance, followed by the sequential deposition of a diffusion barrier layer and the

filling of the patterned trenches with Cu. The excess of Cu can be removed by a chemical mechanical polishing (CMP) process. Among the many deposition methods of Cu, the electrochemical deposition (ED) technique [9][10] has been proven to be the most economic and efficient way to super-fill damascene features without defects, as compared to techniques such as electroless plating, vacuum-based physical vapor deposition (PVD) and chemical vapor deposition (CVD). The atomic layer deposition (ALD) method is another way to generate uniform Cu thin film. Based on sequential layer-by-layer deposition and self-limiting behavior, ALD provides high conformity of thin film quality and accurate control of layer thickness, in spite of the slow deposition rate and low throughput. Inspired by this method, electrochemical atomic layer-by-layer deposition (known as *e*-ALD) has been developed to fabricate ultra-thin Cu film, including two main steps: (1) deposit a sacrificial atomic layer of an appropriate metal by holding an electrode potential within the underpotential deposition region; (2) release the electrode potential to induce the spontaneous displacement of sacrificial metal layer by atomic Cu layer [11]. However, the introduction of copper as interconnects also raises some other challenges, including the degradation of devices due to the diffusion of Cu into the Si and Si-based insulating layers at rather low temperatures [12], the absence of a self-passivized oxide layer causing the corrosion of Cu under chip fabrication process, as well as the poor adhesion between Cu and insulating layers.

To solve these problems, a suitable barrier material with good adhesion to Cu is required to prevent Cu from diffusing into the dielectric layer. The qualified diffusion barrier materials need to be refractory and inactive to both conductors and insulators at rather high temperatures, normally including transition metals such as tantalum (Ta) [13][14][15], tungsten (W) [16][17][18], titanium (Ti) [19][20] and their composites with nitrogen (N), carbon (C) or Si, such as Ta/TaN [21][22][23][24][25], W_2N [26][27][28], TiN [29][30][31][32], TiC [33][34][35], TaSiN [36][37][38], Si_3N_4 [39] and so on. As those state-of-the-art barrier materials are typically poorly conductive, pre-deposition of a Cu seed layer is often needed for the electroplating of Cu, but the Cu seed layer is prone to dissolution in an acidic electrolyte in the subsequent ED process, making it hard to obtain a uniform Cu layer. However, direct plating of uniform Cu film on diffusion barrier materials is of crucial importance in the modern fabrication process. This review briefly summaries the latest development in Cu barrier materials, including state-of-art Ta/TaN, platinum group metals (PGMs) such as ruthenium (Ru)-based materials, 2D materials, self-assembled molecular layers (SAMs) and high-entropy alloys (HEAs). Some of those new barrier materials provide not only reliable Cu diffusion barrier properties during thermal annealing, but also anti-corrosion of Cu in the electrolyte. High-quality ultra-thin film of CVD graphene [40], hexagonal boron nitride (h-BN) [41], magnetron sputtering HEAs [42] and dip-coated SAMs [43] have shown great ability to prevent metals from corrosion in salty solution. In addition, some metal oxide layers (e.g., Ru oxide [44] and Ir oxide [45]) have also been proven as reliable metal corrosion resistants.

2. Cu Interconnects and Diffusion Barrier Materials

Cu interconnects function as internal wiring, connect each circuit compartment and distribute power. In the damascene process, the Cu wiring technique can be vividly demonstrated by the so-called Cu cycle [46] depicted in **Figure 1**, which combines a series of individual processing steps to fabricate a single level of Cu interconnect architecture on a Si wafer.

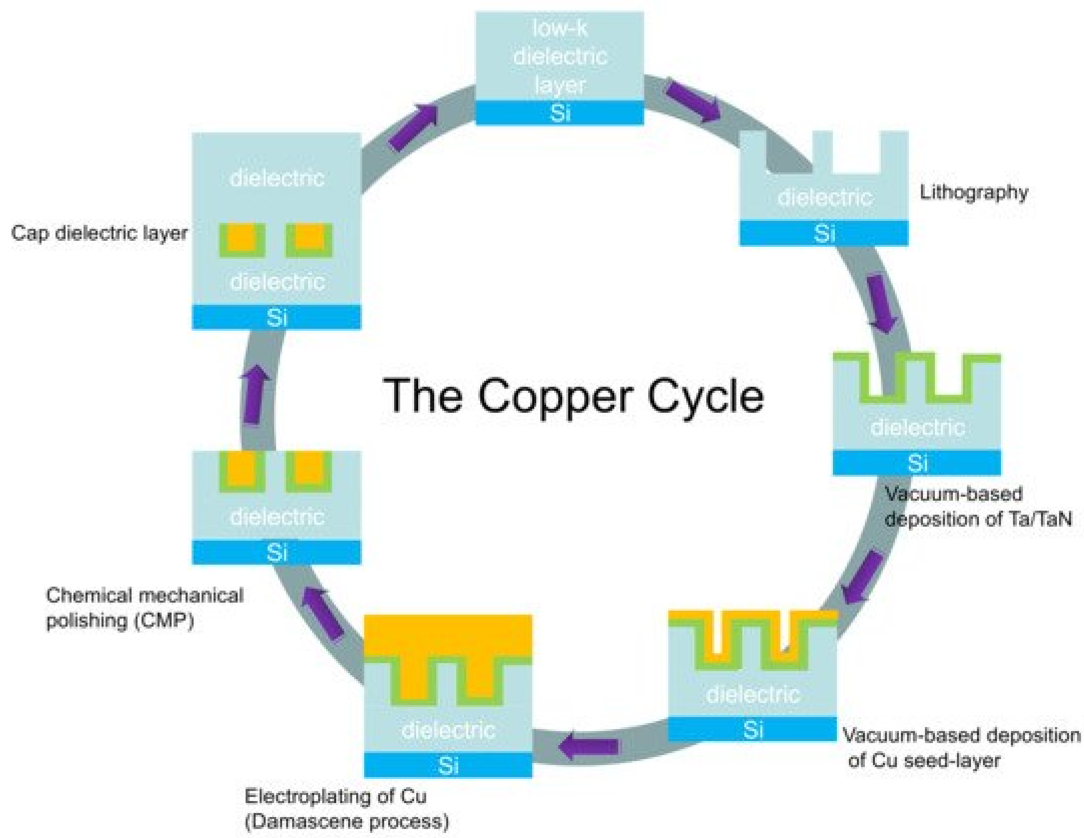

Figure 1. Schematic demonstration of the Cu cycle.

Typically, the Cu cycle starts from the deposition of a low-κ dielectric layer on the Si wafer. Afterwards, the dielectric film is patterned by lithographic method. Then a thin film of Ta/TaN diffusion barrier layer is deposited on top of the dielectric pattern by means of PVD or CVD. Due to the low conductivity and poor nucleation behavior of Cu on the Ta/TaN layer, vacuum deposition of Cu seed-layer is needed to ensure that the following ED process of Cu is able to superfill the damascene features. Finally, a CMP process is conducted to remove the over-plated Cu. The Cu cycle restarts with the deposition of another dielectric layer. During the whole cycle, the defect-free filling of Cu in the damascene trenches is crucial.

However, according to Moore's law [47], the number of transistors in a chip doubles every two years, that is, next generation devices demand the continuous decrease of feature sizes, which as a consequence increases the difficulty of defect-free filling of the trenches in the damascene process. It is well known that the resistances of conventional diffusion barrier materials are too high to be the substrate for direct ED of Cu [48][49][50][51], and an unpleasant phenomenon called "terminal effect" often appears [11][52][53][54][55][56][57][58][59]. This effect becomes more pronounced with the transition from 200 to 300 mm Si wafer. Normally the electrical contact is placed at the periphery of the wafer. When the ED of Cu is performed on a resistive substrate, there is a dramatic IR drop (potential gradient) across the wafer from the contact point to the wafer center, resulting in the non-uniform distribution of current over the resistive substrate with inhomogeneous Cu ED deposition. For this reason, an extra Cu seed layer has to be deposited in advance via PVD [60][61][62][63], CVD [64][65][66][67][68][69], ALD [70][71][72][73] or electroless methods [74][75][76][77][78]. The seed layer prepared by some methods such as PVD or electroless

deposition normally causes undesired “over-hang” at the trench opening, which becomes devastating within the sub-45 nm region and results in unsuccessful filling in the following Cu ED process, as illustrated in **Figure 2** [79].

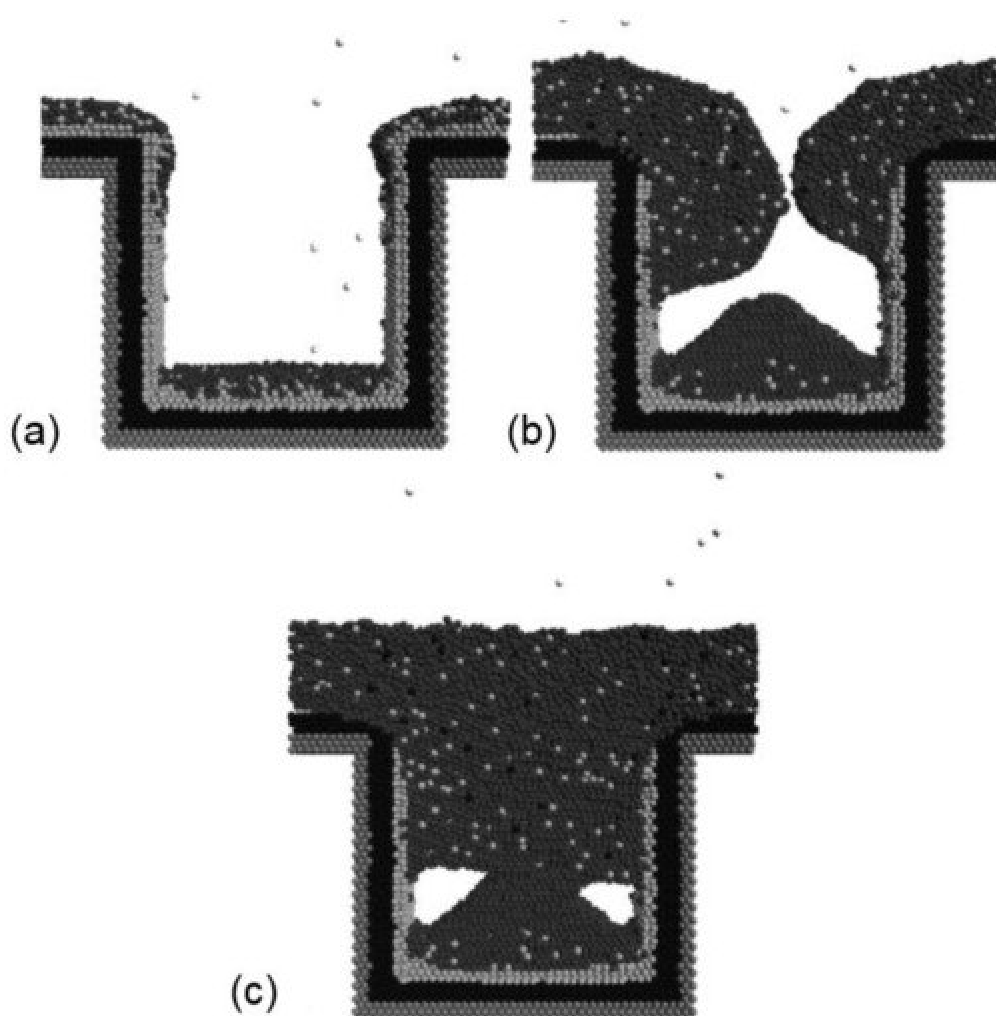

Figure 2. Schematic illustration of the “over-hang” formed by electroless deposition of Cu seed layer, leading to the voids formed by the subsequent electrochemical Cu deposition during a damascene process. (**a**) The formation of Cu overhanging clusters via electroless deposition; (**b**) growth of Cu overhanging clusters during electrochemical Cu deposition; (**c**) failure of Cu super-filling of damascene feature. Reproduced from Hong et al. [79]. Copyright 2005 Elsevier Ltd. All rights reserved.

To avoid this, new barrier materials and techniques must be developed. Desirable characteristics for ideal diffusion barrier materials have been proposed [80][81], including (1) excellent adhesion to Cu metal and dielectric layer; (2) immiscibility with Cu and an ability to prevent Cu diffusion at high temperatures; (3) good conductivity for direct ED of Cu; and (4) simplicity of uniform deposition of ultra-thin film on dielectric layer. In order to find a suitable replacement of traditional barrier materials, attention has been paid to PGM-based materials (e.g., Ru [82][83][84][85], iridium Ir [86][87][88][89], palladium Pd [90] and their composites with other materials [91][92][93][94][95][96][97]), 2D materials (e.g., graphene [98][99], hexagonal boron nitride h-BN [100], and molybdenum disulfide MoS_2 [101][102]), SAMs [103][104][105][106][107] and HEAs [108][109][110][111]. The comparison of properties between new barrier materials

and traditional Ta/TaN is listed in **Table 1**. Compared to Ta/TaN, PGMs (e.g., Ru and Ir) and 2D materials (e.g., graphene) have lower electrical resistivity and comparable melting point. The SAMs' electrical resistivity and melting point strongly depend on their molecular nature, while HEAs have a poor electrical resistivity and their melting point is normally over 1000 °C. SAMs have the easiest deposition method by immersing substrate into the solution containing appropriate molecules. Concerning the layer thickness, 2D materials hold great potential for size downscaling, as single-layer graphene is only one-atom thick.

Table 1. Brief comparison of properties, fabrication methods and expected thickness of barriers.

Barriers	Resistivity (μΩ·cm)	Melting Point (°C)	Deposition Method	Expected Thickness
Ta/TaN	Ta > 13	Ta ~ 2996	PVD or CVD	A few nm
PGMs	Ru ~ 7 Ir ~ 4.7	Ru ~ 2334 Ir ~ 2454	PVD, CVD, ALD, ED, electroless deposition	Few nm
2D materials	Graphene ~ 1	Graphene ~ 3652	CVD	~1 nm
SAMs	/	/	Solution immersion	Monolayer
HEAs	Poor	Normally > 1000	Magnetron sputtering, laser cladding, ED, electron beam evaporation	Few nm

3. Platinum Group Metals (PGM)-Based Materials

Among PGM metals, Ru receives the most attention. It is an air-stable metal with a much lower electrical resistivity (ρ_{Ru} = 7.1 μΩ·cm) [83] compared to that of Ta (ρ_{Ta}= 13 μΩ·cm), which allows the direct electrochemical plating of Cu. More importantly, Ru has a melting point as high as 2334 °C [112], shows negligible solubility [113][114][115] but fantastic wettability with Cu and exhibits excellent adhesion to electroplated Cu at elevated temperatures [82][83][84][85]. Therefore, Ru has been considered as a promising candidate to replace the traditional diffusion barrier materials. Thin films of a Ru barrier layer can be placed on solid substrate via gas phase deposition methods such as PVD, CVD and ALD, or wet deposition methods such as ED and electroless plating. Chyan et al. [84] showed a successful example of the direct ED of a conformal Cu coating layer with controllable thickness on polycrystalline Ru electrode. Annealing up to 600 °C caused no apparent dewetting at the Cu/Ru interface, and more importantly, there was no new phase formed upon further annealing at 800 °C. Chan et al. [85] demonstrated that a high-quality thin film of Cu layer can be formed on top of a 20 nm thin film of Ru deposited on a Si wafer via a standard magnetron sputtering system, showing a Cu ED efficiency as high as 95%. The 20 nm Ru film was sufficient to prevent Cu from diffusing into Si upon annealing at 450 °C for 10 min, but the delamination of Ru thin film from a Si wafer can be seen at 550 °C, resulting in the penetration of Cu into Si substrate. However, reduction of the thickness of Ru layer leads to a decrease in both the Cu ED efficiency and the Cu diffusion-proof temperature. Arunagiri et al. [83] showed that even though a Ru thin film with reduced thickness of 5 nm was able to arrest the diffusion of Cu into Si after annealing at 300 °C for 10 min, only a Cu ED efficiency around 90% was obtained, and a new ruthenium silicide phase was formed at the temperature of 450 °C. Accordingly, a failure mechanism of

Cu/Ru/Si system (**Figure 3**) was proposed by Damayanti et al. [116]. They suggested that the failure appeared at high annealing temperatures and was initiated by the formation of polycrystalline ruthenium silicide, further promoting the diffusion of Cu into Si substrates with the formation of copper silicide protrusions.

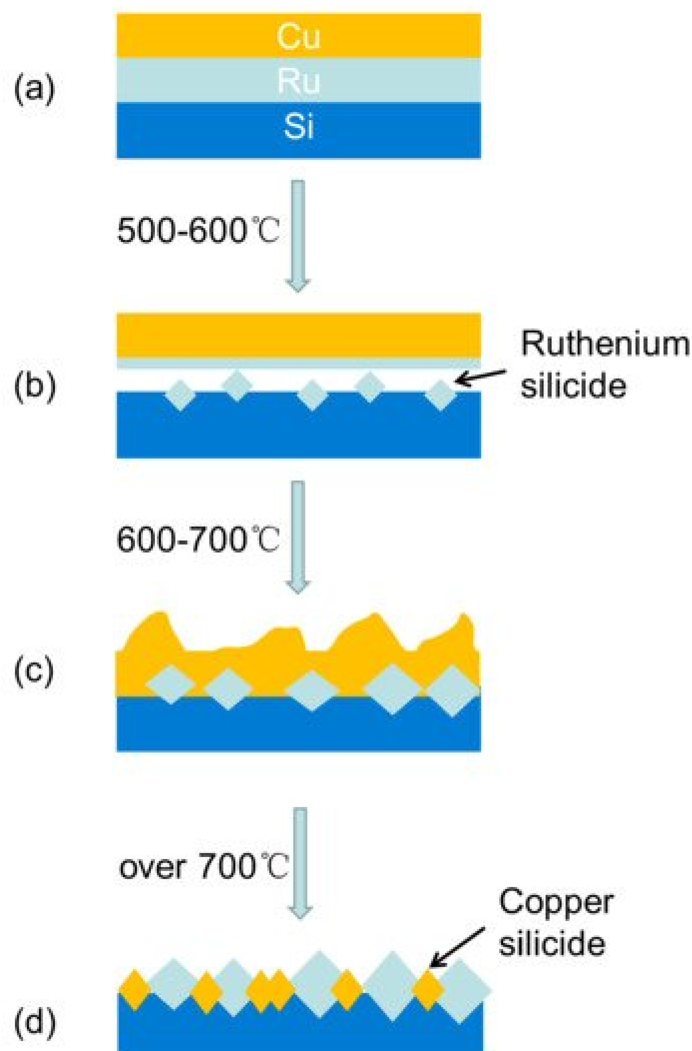

Figure 3. Schematic description of the barrier failure mechanism in Cu/Ru/Si system. (**a**) Intact Ru barrier at the initial stage, (**b**) barrier failure induced by the formation of ruthenium silicide, (**c**) complete dissolution of metallic Ru to form ruthenium silicide, and (**d**) Cu diffusion through ruthenium silicide to form copper silicide.

References

1. Andricacos, P.C. Copper On-Chip Interconnections. Electrochem. Soc. Interface. 1999, 8, 32–37.
2. Li, B.; Sullivan, T.D.; Lee, T.C.; Badami, D. Reliability Challenges for Copper Interconnects. Microelectron. Reliab. 2004, 44, 365–380.
3. Dang, R.L.M.; Shigyo, N. Coupling Capacitances for Two-Dimensional Wires. IEEE Electr. Device 1981, 2, 196–197.

4. Stamper, A.K.; Fuselier, M.B.; Tian, X. Advanced Wiring RC Delay Issues for Sub-0.25-Micron General CMOS. Proc. Int. Interconnet. Tech. Conf. 1998, 62–68.
5. Zuckerman, L. IBM to Make Smaller and Faster Chips. The New York Times, 22 September 1997; D1.
6. Nitta, T.; Ohmi, T.; Otsuki, M.; Takewaki, T.; Shibata, T. Electrical Properties of Giant-Grain Copper Thin Films Formed by a Low Kinetic Energy Particle Process. J. Electrochem. Soc. 1992, 139, 922–927.
7. Hu, C.K.; Harper, J.M.E. Copper Interconnections and Reliability. Mater. Chem. Phys. 1998, 52, 5–16.
8. Zhao, B.; Feiler, D.; Ramanathan, V.; Liu, Q.Z.; Brongo, M.; Wu, J.; Zhang, H.; Kuei, J.C.; Young, D.; Brown, J.; et al. Dual Damascene Interconnect of Copper and Low Permittivity Dielectric for High Performance Integrated Circuits. Electrochem. Solid State Lett. 1998, 1, 276–278.
9. Andricacos, P.; Uzoh, C.; Dukovic, J.; Horkans, J.; Deligianni, H. Damascene Copper Electroplating for Chip Interconnections. IBM. J. Res. Dev. 1998, 42, 567–574.
10. Lizama-Tzec, F.I.; Canché-Canul, L.; Oskam, G. Electrodeposition of Copper into Trenches from a Citrate Plating Bath. Electrochim. Acta. 2011, 56, 9391–9396.
11. Akolkar, R. Current Status and Advances in Damascene Electrodeposition. Encycl. Interfacial Chem. Surf. Sci. Electrochem. Elsevier 2018, 24–31.
12. Chang, C.A. Outdiffusion of Cu through Au: Comparison of (100) and (111) Cu Flms Epitaxially Deposited on Si, and Effects of Annealing Ambients. Appl. Phys. Lett. 1989, 55, 2754–2756.
13. Holloway, K.; Fryer, P.M. Tantalum as a Diffusion Barrier between Copper and Silicon. Appl. Phys. Lett. 1990, 57, 1736–1738.
14. Holloway, K.; Fryer, P.M.; Cabral, C., Jr.; Harper, J.M.E.; Bailey, P.J.; Kelleher, K.H. Tantalum as a Diffusion Barrier between Copper and Silicon: Failure Mechanism and Effect of Nitrogen Additions. J. Appl. Phys. 1992, 71, 5433–5444.
15. Catania, P.; Doyle, J.P.; Cuomo, J.J. Low Resistivity Body-Centered Cubic Tantalum Thin Films as Diffusion Barriers between Copper and Silicon. J. Vac. Sci. Technol. 1992, 10, 3318–3321.
16. Shen, B.W.; Smith, G.C.; Anthony, J.M.; Matyi, R.J. Diffusion Barrier Properties of Thin Selective Chemical Vapor Deposited Tungsten Films. J. Vac. Sci. Technol. 1986, 4, 1369–1376.
17. Park, K.S.; Kim, S. Seedless Copper Electrodeposition onto Tungsten Diffusion Barrier. J. Electrochem. Soc. 2010, 157, D609–D613.
18. Pauleau, Y.; Dassapa, F.C.; Lami, P.; Oberlin, J.C.; Romagna, F. Silicide Formation in Metal/Si Structures and Diffusion Barrier Properties of CVD Tungsten Films. J. Mater. Res. 1989, 4, 156–

162.

19. Ting, C.Y.; Wittmer, M. The Use of Titanium-Based Contact Barrier Layers in Silicon Technology. Thin Solid Films 1982, 96, 327–345.
20. Farahani, M.M.; Turner, T.E.; Barnes, J.J. Evaluation of Titanium as a Diffusion Barrier between Aluminum and Silicon for 1.2 μm CMOS Integrated Circuits. J. Electrochem. Soc. 1987, 134, 2835.
21. Cho, S.L.; Kim, K.B.; Min, S.H.; Shin, H.K.; Kimd, S.D. Diffusion Barrier Properties of Metallorganic Chemical Vapor Deposited Tantalum Nitride Films against Cu Metallization. J. Electrochem. Soc. 1999, 146, 3724.
22. Xie, Q.; Qu, X.P.; Tan, J.J.; Jiang, Y.L.; Zhou, M.; Chen, T.; Ru, G.P. Superior Thermal Stability of Ta/TaN Bi-Layer Structure for Copper Metallization. Appl. Surf. Sci. 2006, 253, 1666–1672.
23. Fréty, N.; Bernard, F.; Nazon, J.; Sarradin, J.; Tedenac, J.C. Copper Diffusion into Silicon Substrates through TaN and Ta/TaN Multilayer Barriers. J. Phase. Equilib. Diff. 2006, 27, 590–597.
24. Bryner, J.; Profunser, D.M.; Vollmann, J.; Mueller, E.; Dual, J. Characterization of Ta and TaN Diffusion Barriers beneath Cu Layers Using Picosecond Ultrasonics. Ultrasonics 2006, 44, e1269–e1275.
25. Yang, L.Y.; Zhang, D.H.; Li, C.Y.; Foo, P.D. Comparative Study of Ta, TaN and Ta/TaN Bi-Layer Barriers for Cu Ultra Low-k Porous Polymer Integration. Thin Solid Films 2004, 462, 176–181.
26. Suh, B.S.; Lee, Y.J.; Hwang, J.S.; Park, C.O. Properties of Reactively Sputtered WNx as Cu Diffusion Barrier. Thin Solid Films 1999, 348, 299–303.
27. Uekubo, M.; Oku, T.; Nii, K.; Murakami, M.; Takahiro, K.; Yamaguchi, S.; Nakano, T.; Ohta, T. WNx Diffusion Barriers between Si and Cu. Thin Solid Films 1996, 286, 170–175.
28. Lee, B.H.; Yong, K. Diffusion Barrier Properties of Metalorganic Chemical Vapor Deposition-WNx Compared with Other Barrier Materials. J. Vac. Sci. Technol. 2004, 22, 2375–2379.
29. Rha, S.K.; Lee, W.J.; Lee, S.Y.; Hwang, Y.S.; Lee, Y.J.; Kim, D.I.; Kim, D.W.; Chun, S.S.; Park, C.O. Improved TiN Film as a Diffusion Barrier between Copper and Silicon. Thin Solid Films 1998, 320, 134–140.
30. Uhm, J.; Jeon, H. TiN Diffusion Barrier Grown by Atomic Layer Deposition Method for Cu Metallization. Jpn. J. Appl. Phys. 2001, 40, 4657–4660.
31. Gagnon, G.; Currie, J.F.; Brebner, J.L.; Darwall, T. Efficiency of TiN Diffusion Barrier between Al and Si Prepared by Reactive Evaporation and Rapid Thermal Annealing. J. Appl. Phys. 1996, 79, 7612–7620.

32. Wang, S.Q.; Raaijmakers, I.; Burrow, B.J.; Suthar, S.; Redkar, S.; Kim, K.B. Reactively Sputtered TiN as a Diffusion Barrier between Cu and Si. J. Appl. Phys. 1990, 68, 5176–5187.
33. Appelbaum, A.; Murarka, S.P. TiC as a Diffusion Barrier between Al and CoSi2. J. Vac. Sci. Technol. 1986, 4, 637–640.
34. Wang, S.J.; Tsai, H.Y.; Sun, S.C. Characterization of Sputtered Titanium Carbide Film as Diffusion Barrier for Copper Metallization. J. Electrochem. Soc. 2001, 148, C563–C568.
35. Eizenberg, M.; Brener, R.; Murarka, S.P. Thermal Stability of the Aluminum/Titanium Carbide/Silicon Contact System. J. Appl. Phys. 1984, 55, 3799–3803.
36. Angyal, M.S.; Shacham-Diamand, Y.; Reid, J.S.; Nicolet, M.A. Performance of Tantalum-Silicon-Nitride Diffusion Barriers between Copper and Silicon Dioxide. Appl. Phys. Lett. 1995, 67, 2152–2154.
37. Hara, T.; Yoshida, Y.; Toida, H. Improved Barrier and Adhesion Properties in Sputtered TaSiN Layer for Copper Interconnects. Electrochem. Solid State Lett. 2002, 5, G36–G39.
38. Girll, A.; Jahnes, C.; Cabral, C. Layered TaSiN as an Oxidation Resistant Electrically Conductive Barrier. J. Mater. Res. 1999, 14, 1604–1609.
39. Klaus, J.W.; Ott, A.W.; Dillon, A.C.; George, S.M. Atomic Layer Controlled Growth of Si3N4 Films Using Sequential Surface Reactions. Surf. Sci. 1998, 418, L14–L19.
40. Raman, R.S.; Banerjee, P.C.; Lobo, D.E.; Gullapalli, H.; Sumandasa, M.; Kumar, A.; Choudhary, L.; Tkacz, R.; Ajayan, P.M.; Majumder, M. Protecting Copper from Electrochemical Degradation by Graphene Coating. Carbon 2012, 50, 4040–4045.
41. Zhang, J.; Yang, Y.; Lou, J. Investigation of Hexagonal Boron Nitride as an Atomically Thin Corrosion Passivation Coating in Aqueous Solution. Nanotechnology 2016, 27, 364004.
42. Zheng, S.J.; Cai, Z.B.; Pu, J.B.; Zeng, C.; Chen, S.Y.; Chen, R.; Wang, L.P. A Feasible Method for the Fabrication of VAlTiCrSi Amorphous High Entropy Alloy Film with Outstanding Anti-Corrosion Property. Appl. Surf. Sci. 2019, 483, 870–874.
43. Yang, W.J.; Li, T.Q.; Zhou, H.H.; Huang, Z.; Fu, C.P.; Chen, L.; Li, M.B.; Kuang, Y.F. Electrochemical and Anti-Corrosion Properties of Octadecanethiol and Benzotriazole Binary Self-Assembled Monolayers on Copper. Electrochim. Acta 2016, 220, 245–251.
44. Fugare, B.Y.; Lokhande, B.J. Study on Structural, Morphological Electrochemical and Corrosion Properties of Mesoporous RuO2 Thin Films Prepared by Ultrasonic Spray Pyrolysis for Supercapacitor Electrode Application. Mat. Sci. Semicon. Proc. 2017, 71, 121–127.
45. Li, M.; Wang, Y.B.; Zhang, X.; Li, Q.H.; Liu, Q.; Cheng, Y.; Zheng, Y.F.; Xi, T.F.; Wei, S.C. Surface Characteristics and Electrochemical Corrosion Behavior of NiTi Alloy Coated with IrO2. Mat. Sci. Eng. 2013, 33, 15–20.

46. Broekmann, P. Tailored Design of Suppressor Ensembles for Damascene and 3D-TSV Copper Plating. In Proceedings of the 12th International Fischer Symposium, Keil, Germany, 4 June 2012.
47. Moore, G.E. Cramming More Components onto Integrated Circuits. Proc. IEEE 1998, 86, 82–85.
48. Fang, J.S.; Chiu, C.F.; Lin, J.H.; Lin, T.Y.; Chin, T.S. Failure Mechanism of 5 nm Thick Ta-Si-C Barrier Layers against Cu Penetration at 700–800 °C. J. Electrochem. Soc. 2009, 156, H147–H152.
49. Kouno, T.; Niwa, H.; Yamada, M. Effect of TiN Microstructure on Diffusion Barrier Properties in Cu Metallization. J. Electrochem. Soc. 1998, 145, 2164–2167.
50. Oku, T.; Kawakami, E.; Uecubo, M.; Takahiro, K.; Yamaguchi, S.; Murakami, M. Diffusion Barrier Property of TaN between Si and Cu. Appl. Surf. Sci. 1996, 99, 265–272.
51. Stavrev, M.; Fischer, D.; Preub, A.; Wenzel, C.; Mattern, N. Study of Nanocrystalline Ta(N,O) Diffusion Barriers for Use in Cu Metallization. Microelectron. Eng. 1997, 33, 269–275.
52. Bisang, J.M.; Kreysa, G. Study of the Effect of Electrode Resistance on Current Density Distribution in Cylindrical Electrochemical Reactors. J. Appl. Electrochem. 1988, 18, 422–430.
53. Lee, J.M.; McCrabb, H.; Taylor, E.J.; Carpio, R. Current Distribution for the Metallization of Resistive Wafer Substrates under Controlled Geometric Variations. J. Electrochem. Soc. 2006, 153, C265–C271.
54. Marshall, S.L.; Wolff, S.K. Analysis of Terminal Effects in Rectangular Electrochemical Cells. Electrochim. Acta 1998, 43, 405–415.
55. Armini, S.; Vereecken, P.M. Impact of “Terminal Effect” on Cu Plating: Theory and Experimental Evidence. ECS Trans. 2010, 25, 185–194.
56. Armini, S. Cu Electrodeposition on Resistive Substrates in Alkaline Chemistry: Effect of Current Density and Wafer RPM. J. Electrochem. Soc. 2011, 158, D390–D394.
57. Choi, J.W.; Guan, O.L.; Mao, Y.J.; Yusoff, H.B.M.; Xie, J.L.; Lan, C.C.; Loh, W.L.; Lau, B.L.; Hong, L.L.H.; Kian, L.G.; et al. TSV Cu Filling Failure Modes and Mechanisms Causing the Failures. IEEE Trans. Comp. Pack. Man. 2014, 4, 581–587.
58. Yang, L.; Atanasova, T.; Radisic, A.; Deconinck, J.; West, A.C.; Vereecken, P. Wafer-Scale Cu Plating Uniformity on Thin Cu Seed Layers. Electrochim. Acta 2013, 104, 242–248.
59. Matlosz, M.; Vallotton, P.H.; West, A.C.; Landolt, D. Nonuniform Current Distribution and Thickness during Electrodeposition onto Resistive Substrates. J. Electrochem. Soc. 1992, 139, 752–761.
60. Sukamto, J.H.; Webb, E.; Andryushchenko, T.; Reid, J. An Evaluation of Electrolytic Repair of Discontinuous PVD Copper Seed Layers in Damascene Vias. J. Appl. Electrochem. 2004, 34,

283–290.

61. Motoyama, K.; van der Straten, O.; Maniscalco, J.; He, M. PVD Cu Reflow Seed Process Optimization for Defect Reduction in Nanoscale Cu/Low-k Dual Damascene Interconnects. J. Electrochem. Soc. 2013, 160, D3211–D3215.
62. Lim, S.T.; Park, Y.C.; Yoo, S.J.; Lee, B.J. Customized Step Coverage of Copper Seed Layer Using Eni-PVD (Energetic Neutral and Ion Physical Vapor Deposition). Thin Solid Films 2009, 517, 3935–3937.
63. Wickramanayaka, S.; Nagahama, H.; Watanabe, E.; Sato, M.; Mizuno, S. Using I-PVD for Copper-Based Interconnects. (Deposition). Solid State Technol. 2002, 45, 67–72.
64. Choi, K.K.; Rhee, S.W. Chemical Vapor Deposition of Copper Film from Hexafluoroacetyl-Acetonate Cu (I) Vinylcyclohexane. Thin Solid Films 2001, 397, 70–77.
65. Shim, K.C.; Lee, H.B.; Kwon, O.K.; Park, H.S.; Koh, W.; Kang, S.W. Bottom-Up Filling of Submicrometer Features in Catalyst-Enhanced Chemical Vapor Deposition of Copper. J. Electrochem. Soc. 2001, 149, G109–G113.
66. Kim, H.; Bhandari, H.B.; Xu, S.; Gordon, R.G. Ultrathin CVD Cu Seed Layer Formation Using Copper Oxynitride Deposition and Room Temperature Remote Hydrogen Plasma Reduction. J. Electrochem. Soc. 2008, 155, H496–H503.
67. Reynolds, S.K.; Smart, C.J.; Baran, E.F.; Baum, T.H.; Larson, C.E.; Brock, P.J. Chemical Vapor Deposition of Copper from 1,5-Cyclooctadiene Copper (I) Hexafluoroacetylacetonate. Appl. Phys. Lett. 1991, 59, 2332–2334.
68. Kröger, R.; Eizenberg, M.; Cong, D.; Yoshida, N.; Chen, L.Y.; Ramaswami, S.; Carl, D. Properties of Copper Films Prepared by Chemical Vapor Deposition for Advanced Metallization of Microelectronic Devices. J. Electrochem. Soc. 1999, 146, 3248.
69. Kwon, O.K.; Lee, H.B.; Kang, S.W.; Park, H.S. Enhancement of the Film Growth Rate by Promoting Iodine Adsorption in the Catalyst-Enhanced Chemical Vapor Deposition of Cu. J. Vac. Sci. Technol. 2002, 20, 408–412.
70. Solanke, R.; Pathangey, B. Atomic Layer Deposition of Copper Seed Layers. Electrochem. Solid State Lett. 2000, 3, 479–480.
71. Moon, D.Y.; Han, D.S.; Shin, S.Y.; Park, J.W.; Kim, B.M.; Kim, J.H. Effects of the Substrate Temperature on the Cu Seed Layer Formed Using Atomic Layer Deposition. Thin Solid Films 2011, 519, 3636–3640.
72. Li, Z.W.; Rahtu, A.; Gordon, R.G. Atomic Layer Deposition of Ultrathin Copper Metal Films from a Liquid Copper (I) Amidinate Precursor. J. Electrochem. Soc. 2006, 153, C787–C794.

73. Kalutarage, L.C.; Clendenning, S.B.; Winter, C.H. Low-Temperature Atomic Layer Deposition of Copper Films Using Borane Dimethylamine as the Reducing Co-Reagent. Chem. Mater. 2014, 26, 3731–3738.
74. Lee, C.H.; Hwang, S.; Kim, S.C.; Kim, J.J. Cu Electroless Deposition onto Ta Substrates: Application to Create a Seed Layer for Cu Electrodeposition. Electrochem. Solid State Lett. 2006, 9, C157–C160.
75. Aithal, R.K.; Yenamandra, S.; Gunasekaran, R.A.; Coane, P.; Varahramyan, K. Electroless Copper Deposition on Silicon with Titanium Seed Layer. Mater. Chem. Phys. 2006, 98, 95–102.
76. Chong, S.P.; Ee, Y.C.; Chen, Z.; Law, S.B. Electroless Copper Seed Layer Deposition on Tantalum Nitride Barrier Film. Surf. Coat. Technol. 2005, 198, 287–290.
77. Wang, Z.; Yaegashi, O.; Sakaue, H.; Takahagi, T.; Shingubara, S. Highly Adhesive Electroless Cu Layer Formation Using an Ultra-Thin Ionized Cluster Beam (ICB)-Pd Catalytic Layer for Sub-100 nm Cu Interconnections. Jpn. J. Appl. Phys. 2003, 42, L1223–L1225.
78. Hsu, H.H.; Teng, C.W.; Lin, S.J.; Yeh, J.W. Sn/Pd Catalyzation and Electroless Cu Deposition on TaN Diffusion Barrier Layers. J. Electrochem. Soc. 2002, 149, C143–C149.
79. Hong, R.T.; Huang, M.J.; Yang, J.Y. Molecular Dynamics Study of Copper Trench Filling in Damascene Process. Mat. Sci. Semicon. Proc. 2005, 8, 587–601.
80. Nicolet, M.A. Diffusion Barriers in Thin Films. Thin Solid Films 1978, 52, 415–443.
81. Pillai, K.S.M. Copper Electrodeposition on Ruthenium-Tantalum and Corrosion of Plasma Treated Copper in Post Etch Cleaning Solution; University of North Texas: Denton, TX, USA, 2011.
82. Kim, H.; Koseki, T.; Ohba, T.; Ohta, T.; Kojima, Y.; Sato, H.; Shimogaki, Y. Cu Wettability and Diffusion Barrier Property of Ru Thin Film for Cu Metallization. J. Electrochem. Soc. 2005, 152, G594–G600.
83. Arunagiri, T.N.; Zhang, Y.; Chyan, O.; El-Bouanani, M.; Kim, M.J.; Chen, K.H.; Wu, C.T.; Chen, L.C. 5 nm Ruthenium Thin Film as a Directly Plateable Copper Diffusion Barrier. Appl. Phys. Lett. 2005, 86, 083104–083106.
84. Chyan, O.; Arunagiri, T.N.; Ponnuswamy, T. Electrodeposition of Copper Thin Film on Ruthenium: A Potential Diffusion Barrier for Cu Interconnects. J. Electrochem. Soc. 2003, 150, C347–C350.
85. Chan, R.; Arunagiri, T.N.; Zhang, Y.; Chyan, O.; Wallace, R.M.; Kim, M.J.; Hurd, T.Q. Diffusion Studies of Copper on Ruthenium Thin Film: A Plateable Copper Diffusion Barrier. Electrochem. Solid State Lett. 2004, 7, G154–G157.
86. Lim, Y.H.; Yoo, H.; Choi, B.H.; Lee, J.H.; Lee, H.N.; Lee, H.K. Atomic-Layer-Deposited Ir Thin Film as a Novel Diffusion Barrier Layer in Cu Interconnection. Phys. Status Solidi. 2011, 8, 891–894.

87. Choi, B.H.; Lee, J.H.; Lee, H.K.; Kim, J.H. Effect of Interface Layer on Growth Behavior of Atomic-Layer-Deposited Ir Thin Film as Novel Cu Diffusion Barrier. Appl. Surf. Sci. 2011, 257, 9654–9660.

88. Song, S.I.; Lee, J.H.; Choi, B.H.; Lee, H.K.; Shin, D.C.; Lee, J.W. Hydrogen-Plasma-Assisted Hybrid Atomic Layer Deposition of Ir Thin Film as Novel Cu Diffusion Barrier. Surf. Coat. Technol. 2012, 211, 14–17.

89. Josell, D.; Bonevich, J.; Moffat, T.; Aaltonen, T.; Ritala, M.; Leskelä, M. Iridium Barriers for Direct Copper Electrodeposition in Damascene Processing. Electrochem. Solid State Lett. 2006, 9, C48–C50.

90. Chow, K.M.; Ng, W.Y.; Yeung, L.K. Barrier Properties of Ni, Pd and Pd-Fe for Cu Diffusion. Surf. Coat. Technol. 1998, 105, 56–64.

91. Kim, Y.S.; Kim, H.I.; Cho, J.H.; Seo, H.K.; Dar, M.A.; Shin, H.S.; Eyck, G.A.T.; Lu, T.M.; Senkevich, J.J. Electroless Copper on Refractory and Noble Metal Substrates with an Ultra-Thin Plasma-Assisted Atomic Layer Deposited Palladium Layer. Electrochim. Acta 2006, 51, 2400–2406.

92. Leu, L.C.; Norton, D.P.; McElwee-White, L.; Anderson, T.J. Ir/TaN as a Bilayer Diffusion Barrier for Advanced Cu Interconnects. Appl. Phys. Lett. 2008, 92, 111917–111919.

93. De Reus, R.; Koper, R.J.I.M.; Zeijlemaker, H.; Saris, F.W. Stability of Amorphous Ir-Ta Diffusion Barriers between Cu and Si. Mater. Lett. 1990, 9, 500–503.

94. Yang, C.C.; Cohen, S.; Shaw, T.; Wang, P.C.; Nogami, T.; Edelstein, D. Characterization of “Ultrathin-Cu”/Ru (Ta)/TaN Liner Stack for Copper Interconnects. IEEE Trans. Electr. Device 2010, 31, 722–724.

95. Kondati Natarajan, S.; Nies, C.L.; Nolan, M. Ru Passivated and Ru Doped ε-TaN Surfaces as Combined Barrier and Liner Material for Copper Interconnects: A First Principles Study. J. Mater. Chem. 2019, 7, 7959–7973.

96. Tan, J.J.; Qu, X.P.; Xie, Q.; Zhou, Y.; Ru, G.P. The Properties of Ru on Ta-Based Barriers. Thin Solid Films 2006, 504, 231–234.

97. Li, J.; Lu, H.S.; Wang, Y.W.; Qu, X.P. Sputtered Ru–Ti, Ru–N and Ru–Ti–N Films as Cu Diffusion Barrier. Microelectron. Eng. 2011, 88, 635–640.

98. Zhao, Y.; Liu, Z.; Sun, T.; Zhang, L.; Jie, W.; Wang, X.; Xie, Y.; Tsang, Y.; Long, H.; Chai, Y. Mass Transport Mechanism of Cu Species at the Metal/Dielectric Interfaces with a Graphene Barrier. ACS Nano 2014, 8, 12601–12611.

99. Lee, H.C.; Jo, M.; Lim, H.; Yoo, M.S.; Lee, E.; Nguyen, N.N.; Han, S.Y.; Cho, K. Toward Near-Bulk Resistivity of Cu for Next-Generation Nano-Interconnects: Graphene-Coated Cu. Carbon 2019,

149, 656–663.

100. Zhao, L.; Lofrano, M.; Croes, K.; Van Besien, E.; Tőkei, Z.; Wilson, C.J.; Degraeve, R.; Kauerauf, T.; Beyer, G.P.; Claeys, C. Evaluations of Intrinsic Time Dependent Dielectric Breakdown of Dielectric Copper Diffusion Barriers. Thin Solid Films 2011, 520, 662–666.
101. Nies, C.L.; Nolan, M. DFT Calculations of the Structure and Stability of Copper Clusters on MoS2. Beilstein. J. Nanotech. 2020, 11, 391–406.
102. Jing, D.; Lii-Rosales, A.; Lai, K.C.; Li, Q.; Kim, J.; Tringides, M.C.; Evans, J.W.; Thiel, P.A. Non-Equilibrium Growth of Metal Clusters on a Layered Material: Cu on MoS2. New J. Phys. 2020, 22, 053033.
103. Ramanath, G.; Cui, G.; Ganesan, P.G.; Guo, X.; Ellis, A.V.; Stukowski, M.; Doppelt, P.; Lane, M. Self-Assembled Subnanolayers as Interfacial Adhesion Enhancers and Diffusion Barriers for Integrated Circuits. Appl. Phys. Lett. 2003, 83, 383–385.
104. Khaderbad, M.A.; Pandharipande, R.; Singh, V.; Madhu, S.; Ravikanth, M.; Rao, V.R. Porphyrin Self-Assembled Monolayer as a Copper Diffusion Barrier for Advanced CMOS Technologies. IEEE Trans. Electron. Dev. 2012, 59, 1963–1969.
105. Liu, X.; Wang, Q.; Wu, S.; Liu, Z. Enhanced CVD of Copper Films on Self-Assembled Monolayers as Ultrathin Diffusion Barriers. J. Electrochem. Soc. 2006, 153, C142–C145.
106. Caro, A.M.; Armini, S.; Richard, O.; Maes, G.; Borghs, G.; Whelan, C.M.; Travaly, Y. Bottom-Up Engineering of Subnanometer Copper Diffusion Barriers Using NH2-Derived Self-Assembled Monolayers. Adv. Funct. Mater. 2010, 20, 1125–1131.
107. Kong, Z.; Wang, Q.; Ding, L.; Wu, T. Study on Chemical Vapor Deposited Copper Films on Cyano and Carboxylic Self-Assembled Monolayer Diffusion Barriers. Thin Solid Films 2010, 518, 4852–4859.
108. Tsai, M.H.; Wang, C.W.; Lai, C.H.; Yeh, J.W.; Gan, J.Y. Thermally Stable Amorphous (AlMoNbSiTaTiVZr)50N50 Nitride Film as Diffusion Barrier in Copper Metallization. Appl. Phys. Lett. 2008, 92, 052109.
109. Li, R.; Li, M.; Jiang, C.; Qiao, B.; Zhang, W.; Xu, J. Thermal Stability of AlCrTaTiZrMo-Nitride High Entropy Film as a Diffusion Barrier for Cu Metallization. J. Alloys Compd. 2019, 773, 482–489.
110. Chang, S.Y.; Wang, C.Y.; Li, C.E.; Huang, Y.C. 5 nm-Thick (AlCrTaTiZrRu)N0.5 Multi-Component Barrier Layer with High Diffusion Resistance for Cu Interconnects. Nanosci. Nanotech. Lett. 2011, 3, 289–293.
111. Chang, S.Y.; Chen, M.K.; Chen, D.S. Multiprincipal-Element AlCrTaTiZr-Nitride Nanocomposite Film of Extremely High Thermal Stability as Diffusion Barrier for Cu Metallization. J. Electrochem. Soc. 2009, 156, G37–G42.

112. Steeves, M.M. Electronic Transport Properties of Ruthenium and Ruthenium Dioxide Thin Films. In Electronic Theses and Dissertations; University of Maine: Orono, ME, USA, 2011; Available online: https://digitalcommons.library.umaine.edu/etd/262 (accessed on 15 October 2020).
113. Park, C.; Bauer, E.; Poppa, H. A Re-Examination of the Cu/Ru (0001) System. Surf. Sci. 1987, 187, 86–97.
114. Chu, J.P.; Lin, C.H.; John, V.S. Cu Films Containing Insoluble Ru and RuNx on Barrierless Si for Excellent Property Improvements. Appl. Phys. Lett. 2007, 91, 132109–132111.
115. Kim, K.H.; Lim, T.; Park, K.J.; Koo, H.C.; Kim, M.J.; Kim, J.J. Investigation of Cu Growth Phenomena on Ru Substrate During Electroless Deposition Using Hydrazine as a Reducing Agent. Electrochim. Acta 2015, 151, 249–255.
116. Damayanti, M.; Sritharan, T.; Mhaisalkar, S.G.; Phoon, E.; Chan, L. Study of Ru Barrier Failure in the Cu/Ru/Si System. J. Mater. Res. 2007, 22, 2505–2511.

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