

Takagi–Sugeno Fuzzy-PI Controller Hardware

Subjects: [Engineering, Electrical & Electronic](#) | [Computer Science, Artificial Intelligence](#)

Contributor: Sérgio N. Silva , Felipe F. Lopes , Carlos Valderrama , Marcelo A. C. Fernandes

The intelligent system Field Programmable Gate Array (FPGA) is represented as Takagi–Sugeno Fuzzy-PI controller. The implementation uses a fully parallel strategy associated with a hybrid bit format scheme (fixed-point and floating-point). Two hardware designs are proposed; the first one uses a single clock cycle processing architecture, and the other uses a pipeline scheme. The bit accuracy was tested by simulation with a nonlinear control system of a robotic manipulator. The area, throughput, and dynamic power consumption of the implemented hardware are used to validate and compare the results of this proposal. The results achieved allow the use of the proposed hardware in applications with high-throughput, low-power, and ultra-low-latency requirements such as teleoperation of robot manipulators, tactile internet, or industry 4.0 automation, among others.

[FPGA](#)

[Hardware](#)

[Takagi-Sugeno](#)

[Fuzzy](#)

[Fuzzy-PI](#)

1. Introduction

Systems based on Fuzzy Logic (FL), have been used in many industrial and commercial applications such as robotics, automation, control, and classification problems. Unlike high data volume systems, such as Big Data and Mining of Massive Datasets (MMD) [\[1\]](#)[\[2\]](#)[\[3\]](#), one of the great advantages of Fuzzy Logic is its ability to work with incomplete or inaccurate information.

Intelligent systems based on production rules that use Fuzzy Logic in the inference process are called in the literature Fuzzy Systems (FS) [\[4\]](#). Among the existing inference strategies, the most used, the Mamdani and the Takagi–Sugeno, are differentiated by the final stage of the inference process [\[5\]](#)[\[6\]](#)[\[7\]](#)[\[8\]](#)[\[9\]](#)[\[10\]](#)[\[11\]](#)[\[12\]](#)[\[13\]](#)[\[14\]](#)[\[15\]](#)[\[16\]](#)[\[17\]](#)[\[18\]](#)[\[19\]](#)[\[20\]](#).

2. Development

The interest in the development of dedicated hardware implementing Fuzzy Systems has increased due to the demand for high-throughput, low-power, and ultra-low-latency control systems for emerging applications such as the tactile Internet [\[21\]](#)[\[22\]](#), the Internet of Things (IoT), and Industry 4.0, where the problems associated with processing, power, latency, and miniaturization are fundamental. Robotic manipulators used on the tactile internet need a high-throughput and ultra-low-latency control system, and this can be achieved with dedicated hardware [\[21\]](#).

The development of dedicated hardware, in addition to speeding up parallel processing, makes it possible to operate with clocks adapted to low-power consumption [23][24][25][26][27][28][29]. The works presented in [30][31][32][33][34][35][36][37] propose implementations of FS on reconfigurable hardware (Field Programmable Gate Array—FPGA), showing the possibilities associated with the acceleration of fuzzy inference processes having a high degree of parallelization. Other works propose specific implementations of Fuzzy Control Systems (FCS) using the Fuzzy Mamdani Inference Machine (M-FIM) and the Takagi–Sugeno Fuzzy Inference Machine (TS-FIM) [5][6][7][8][9][10][11][12][13][14][15][16][17][18][19][20]. The works presented in [38][39][40] propose the Takagi–Sugeno hardware acceleration for other types of application fields.

References

1. Poli, V.S.R. Fuzzy data mining and web intelligence. In Proceedings of the 2015 International Conference on Fuzzy Theory and Its Applications (iFUZZY), Yilan, Taiwan, 18–20 November 2015; pp. 74–79. [Google Scholar]
2. Nasrollahzadeh, A.; Karimian, G.; Mehrafsa, A. Implementation of neuro-fuzzy system with modified high performance genetic algorithm on embedded systems. *Appl. Soft Comput.* 2017. [Google Scholar] [CrossRef]
3. Yaqoob, I.; Hashem, I.A.T.; Gani, A.; Mokhtar, S.; Ahmed, E.; Anuar, N.B.; Vasilakos, A.V. Big data: From beginning to future. *Int. J. Inf. Manag.* 2016, 36, 1231–1247. [Google Scholar] [CrossRef]
4. Oviedo, J.; Vandewalle, J.; Wertz, V. *Fuzzy Logic, Identification and Predictive Control*; Springer: London, UK, 2004. [Google Scholar]
5. Aguilar, A.; Pérez, M.; Camas, J.L.; Hernández, H.R.; Ríos, C. Efficient Design and Implementation of a Multivariate Takagi-Sugeno Fuzzy Controller on an FPGA. In Proceedings of the 2014 International Conference on Mechatronics, Electronics and Automotive Engineering, Cuernavaca, Mexico, 18–21 November 2014; pp. 152–157. [Google Scholar] [CrossRef]
6. Hassan, L.H.; Moghavvemi, M.; Almurib, H.A.F.; Muttaqi, K.M. Damping of low-frequency oscillations using Takagi-Sugeno Fuzzy stabilizer in real-time. In Proceedings of the 2016 IEEE Industry Applications Society Annual Meeting, Portland, OR, USA, 2–6 October 2016; pp. 1–7. [Google Scholar] [CrossRef]
7. Boncalo, O.; Amaricai, A.; Lendek, Z. Configurable Hardware Accelerator Architecture for a Takagi-Sugeno Fuzzy Controller. In Proceedings of the 2019 22nd Euromicro Conference on Digital System Design (DSD), Kallithea, Greece, 28–30 August 2019; pp. 96–101. [Google Scholar] [CrossRef]

8. Bicakci, S. On the Implementation of Fuzzy VMC for an Under Actuated System. *IEEE Access* 2019, 7, 163578–163588. [Google Scholar] [CrossRef]
9. Banjanovic-Mehmedovic, L.; Husejnovic, A. FPGA based Hexapod Robot Navigation using Arbitration of Fuzzy Logic Controlled Behaviors. In Proceedings of the 2019 XXVII International Conference on Information, Communication and Automation Technologies (ICAT), Sarajevo, Bosnia and Herzegovina, 20–23 October 2019; pp. 1–6. [Google Scholar] [CrossRef]
10. Akbatı, O.; Üzgün, H.D.; Akkaya, S. Hardware-in-the-loop simulation and implementation of a fuzzy logic controller with FPGA: Case study of a magnetic levitation system. *Trans. Inst. Meas. Control.* 2019, 41, 2150–2159. [Google Scholar] [CrossRef]
11. Sánchez-Solano, S.; Brox, M.; del Toro, E.; Brox, P.; Baturone, I. Model-Based Design Methodology for Rapid Development of Fuzzy Controllers on FPGAs. *IEEE Trans. Ind. Informatics* 2013, 9, 1361–1370. [Google Scholar] [CrossRef]
12. Sánchez-Solano, S.; del Toro, E.; Brox, M.; Baturone, I.; Barriga, Á. A design environment for synthesis of embedded fuzzy controllers on FPGAs. In Proceedings of the International Conference on Fuzzy Systems, Barcelona, Spain, 18–23 July 2010; pp. 1–8. [Google Scholar] [CrossRef]
13. Baturone, I.; Moreno-Velo, F.J.; Sanchez-Solano, S.; Ollero, A. Automatic design of fuzzy controllers for car-like autonomous robots. *IEEE Trans. Fuzzy Syst.* 2004, 12, 447–465. [Google Scholar] [CrossRef]
14. Youssef, A.; Telbany, M.E.; Zekry, A. Reconfigurable generic FPGA implementation of fuzzy logic controller for MPPT of PV systems. *Renew. Sustain. Energy Rev.* 2018, 82, 1313–1319. [Google Scholar] [CrossRef]
15. Khati, H.; Mellah, R.; Talem, H. Neuro-fuzzy Control of a Position-Position Teleoperation System Using FPGA. In Proceedings of the 2019 24th International Conference on Methods and Models in Automation and Robotics (MMAR), Międzyzdroje, Poland, 26–29 August 2019; pp. 64–69. [Google Scholar] [CrossRef]
16. Sun, Y.; Tang, S.; Meng, Z.; Zhao, Y.; Yang, Y. A scalable accuracy fuzzy logic controller on {FPGA}. *Expert Syst. Appl.* 2015, 42, 6658–6673. [Google Scholar] [CrossRef]
17. Deliparaschos, K.M.; Nenedakis, F.I.; Tzafestas, S.G. Design and Implementation of a Fast Digital Fuzzy Logic Controller Using FPGA Technology. *J. Intell. Robot. Syst.* 2006, 45, 77–96. [Google Scholar] [CrossRef]
18. de la Cruz-Alejo, J.; Antonio-Méndez, R.; Salazar-Pereyra, M. Fuzzy logic control on FPGA for two axes solar tracking. *Neural Comput. Appl.* 2019, 31, 2469–2483. [Google Scholar] [CrossRef]
19. Huang, H.C.; Tao, C.W.; Chuang, C.C.; Xu, J.J. FPGA-Based Mechatronic Design and Real-Time Fuzzy Control with Computational Intelligence Optimization for Omni-Mecanum-Wheeled

- Autonomous Vehicles. *Electronics* 2019, 8, 1328. [Google Scholar] [CrossRef]
20. Krim, S.; Gdaim, S.; Mtibaa, A.; Mimouni, M.F. Contribution of the FPGAs for Complex Control Algorithms: Sensorless DTFC with an EKF of an Induction Motor. *Int. J. Autom. Comput.* 2019, 16, 226–237. [Google Scholar] [CrossRef]
21. Junior, J.C.V.S.; Torquato, M.F.; Noronha, D.H.; Silva, S.N.; Fernandes, M.A.C. Proposal of the Tactile Glove Device. *Sensors* 2019, 19, 5029. [Google Scholar] [CrossRef] [PubMed]
22. Simsek, M.; Ajiaz, A.; Dohler, M.; Sachs, J.; Fettweis, G. The 5G-Enabled Tactile Internet: Applications, requirements, and architecture. In Proceedings of the 2016 IEEE Wireless Communications and Networking Conference, Doha, Qatar, 3–6 April 2016; pp. 1–6. [Google Scholar] [CrossRef]
23. Torquato, M.F.; Fernandes, M.A.C. High-Performance Parallel Implementation of Genetic Algorithm on FPGA. *Circuits Syst. Signal Process.* 2019, 38, 4014–4039. [Google Scholar] [CrossRef]
24. Da Costa, A.L.X.; Silva, C.A.D.; Torquato, M.F.; Fernandes, M.A.C. Parallel Implementation of Particle Swarm Optimization on FPGA. *IEEE Trans. Circuits Syst. II Express Briefs* 2019, 66, 1875–1879. [Google Scholar] [CrossRef]
25. Silva, L.M.D.D.; Torquato, M.F.; Fernandes, M.A.C. Parallel Implementation of Reinforcement Learning Q-Learning Technique for FPGA. *IEEE Access* 2019, 7, 2782–2798. [Google Scholar] [CrossRef]
26. Coutinho, M.G.F.; Torquato, M.F.; Fernandes, M.A.C. Deep Neural Network Hardware Implementation Based on Stacked Sparse Autoencoder. *IEEE Access* 2019, 7, 40674–40694. [Google Scholar] [CrossRef]
27. Blaiech, A.G.; Khalifa, K.B.; Valderrama, C.; Fernandes, M.A.; Bedoui, M.H. A Survey and Taxonomy of FPGA-based Deep Learning Accelerators. *J. Syst. Archit.* 2019, 98, 331–345. [Google Scholar] [CrossRef]
28. Lopes, F.F.; Ferreira, J.C.; Fernandes, M.A.C. Parallel Implementation on FPGA of Support Vector Machines Using Stochastic Gradient Descent. *Electronics* 2019, 8, 631. [Google Scholar] [CrossRef]
29. Noronha, D.H.; Torquato, M.F.; Fernandes, M.A. A parallel implementation of sequential minimal optimization on FPGA. *Microprocess. Microsyst.* 2019, 69, 138–151. [Google Scholar] [CrossRef]
30. Chowdhury, S.R.; Saha, H. A High-Performance FPGA-Based Fuzzy Processor Architecture for Medical Diagnosis. *IEEE Micro* 2008, 28, 38–52. [Google Scholar] [CrossRef]
31. Ontiveros-Robles, E.; Gonzalez-Vazquez, J.L.; Castro, J.R.; Castillo, O. A hardware architecture for real-time edge detection based on interval type-2 fuzzy logic. In Proceedings of the 2016 IEEE

- International Conference on Fuzzy Systems (FUZZ-IEEE), Vancouver, BC, Canada, 24–29 July 2016; pp. 804–810. [Google Scholar] [CrossRef]
32. Prado, R.N.A.; Melo, J.D.; Oliveira, J.A.N.; Dória Neto, A.D. FPGA based implementation of a Fuzzy Neural Network modular architecture for embedded systems. In Proceedings of the 2012 International Joint Conference on Neural Networks (IJCNN), Brisbane, QLD, Australia, 10–15 June 2012; pp. 1–7. [Google Scholar] [CrossRef]
33. Loan, S.A.; Murshid, A.M. A novel VLSI architecture of a multi membership function based MAX-MIN calculator circuit. In Proceedings of the 2013 International Conference on Advanced Electronic Systems (ICAES), Pilani, India, 21–23 September 2013; pp. 74–78. [Google Scholar] [CrossRef]
34. Loan, S.A.; Murshid, A.M.; Abbasi, S.A.; Alamoud, A.R.M. A Novel VLSI Architecture for a Fuzzy Inference Processor Using Gaussian-Shaped Membership Function. *J. Intell. Fuzzy Syst.* 2013, 24, 5–19. [Google Scholar] [CrossRef]
35. Titinchi, A.A.; Halasa, N. FPGA implementation of simplified Fuzzy LRU replacement algorithm. In Proceedings of the 2019 16th International Multi-Conference on Systems, Signals Devices (SSD), Istanbul, Turkey, 21–24 March 2019; pp. 657–662. [Google Scholar] [CrossRef]
36. Zavala, A.H.; Nieto, O.C. Fuzzy Hardware: A Retrospective and Analysis. *IEEE Trans. Fuzzy Syst.* 2012, 20, 623–635. [Google Scholar] [CrossRef]
37. Bosque, G.; del Campo, I.; Echanobe, J. Fuzzy systems, neural networks and neuro-fuzzy systems: A vision on their hardware implementation and platforms over two decades. *Eng. Appl. Artif. Intell.* 2014, 32, 283–331. [Google Scholar] [CrossRef]
38. Tchendjou, G.T.; Simeu, E.; Alhakim, R. Fuzzy logic based objective image quality assessment with FPGA implementation. *J. Syst. Archit.* 2018, 82, 24–36. [Google Scholar] [CrossRef]
39. Liviu, T. FPGA Implementation of a Fuzzy Rule Based Contrast Enhancement System for Real Time Applications. In Proceedings of the 2018 22nd International Conference on System Theory, Control and Computing (ICSTCC), Sinaia, Romania, 10–12 October 2018; pp. 117–122. [Google Scholar] [CrossRef]
40. Júnior, E.I.; Manuel Garcés Socarrás, L.; Pimenta, T.C. Design and low-cost FPGA implementation of the fuzzy decision system. In Proceedings of the 2018 30th International Conference on Microelectronics (ICM), Sousse, Tunisia, 16–19 December 2018; pp. 291–294.

Retrieved from <https://www.encyclopedia.pub/entry/history/show/7989>