Recent Trends in Copper Metallization

Subjects: Engineering, Electrical & Electronic

Contributor: Hyung-Woo Kim

The Cu/low-k damascene process was introduced to alleviate the increase in the RC delay of Al/SiO_2 interconnects, but now that the technology generation has reached 1× nm or lower, a number of limitations have become apparent. Due to the integration limit of low-k materials, the increase in the RC delay due to scaling can only be suppressed through metallization.

Keywords: BEOL ; interconnect ; copper ; low-k ; metallization

1. Introduction

Continuous developments in integrated chip scaling have improved circuit density and chip performance in recent decades. Moore's law, which states that the number of transistors on a microchip doubles every two years, is now accepted as an empirical law. These advances have been achieved not only with simple reductions in dimensions; they have also been spurred by new patterning approaches, innovative device architectures, tool improvements, design–technology co-optimization, and the integration of new materials [1][2].

The increasing number of transistors on an integrated chip usually leads to an increase in the complexity of the interconnections. This can be resolved by increasing the number of vertical stacking levels based on hierarchical wiring schemes for effective design allocation [3][4]. A hierarchical wiring system is commonly constructed by vertically distributing various metal levels with different minimum pitches. Depending on their purpose, these interconnects can be divided into three groups: local, intermediate, or global interconnects.

Local interconnects: The minimum metal pitch is applied to the levels closest to the transistor. They adopt state-of-the-art processes and technologies with low-k dielectrics and metallization to minimize the resistance−capacitance (RC) delay, which is most affected by patterning.

Intermediate interconnects: They connect primitive cells or signal transmission, such as the system clock. Because the congestion is lower than for local interconnects, a relaxed metal pitch and an increase in thickness are allowed.

Global interconnects: These are the wiring levels at the top of the integrated chip and are used to minimize the power transmission and voltage drop. They typically have a thick metal layer and a relaxed pitch. However, they are subject to additional requirements related to connections with the outside of the chip, i.e., the packaging.

2. Metallization

A typical DD Cu line is surrounded by a barrier, a liner, and a cap (**Figure 1**) [5]. The barrier promotes metal adhesion to the dielectric, protects Cu from oxidation, and acts as a nucleation layer for the liner metals. The liner facilitates Cu seeding and the plating process and, more importantly, improves the Cu interface for the suppression of EM. After the emergence of 14 nm technology, a metal cap was applied to the top of the line to improve for EM performance due to the small volume of Cu [6]. A diffusion barrier is required to prevent the Cu from mixing with the surrounding dielectric material when manufacturing a Cu interconnect with a damascene structure. The barrier layer reduces the cross-sectional area of the interconnect, and the effective resistance of the Cu line becomes higher than that of a barrier-free Cu line. The increase in resistivity due to the barrier increases significantly when the width of the interconnect line is reduced. According to Matthiessen's law, line resistivity consists of bulk resistivity, impurity scattering, surface scattering, and GB scattering [7][8]. Before the emergence of 7 nm technology, bulk resistivity and impurity scattering usually determined line resistivity. However, since then, surface scattering and particle boundary scattering have taken on greater importance. For surface scattering, it is essential to minimize the volume fraction of Cu occupied by the barrier and liner, while particle boundary scattering is likely to affect scattering at the interface and the Cu grain size.

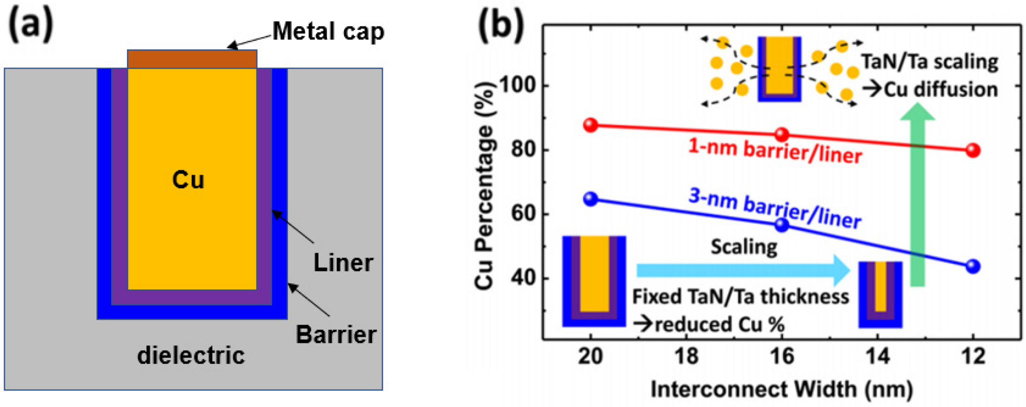

Figure 1. (**a**) Typical metallization of a Cu line with a barrier, liner, and metal cap. (**b**) Scaling challenges for the barrier and liner; in particular, a lower cross-sectional area is occupied by Cu with scaling [5].

2.1. TaN Barrier/Liner Scaling

In order to maximize the Cu volume fraction, the TaN/Ta liner thickness must be reduced. In addition, the thickness of the Cu seed needs to be reduced to prevent the top pinch-off shape during subsequent Cu electroplating. However, the nonconformal step coverage of PVD results in gap-fill problems caused by the overhang and high resistance due to the thick barrier at the via bottom. Therefore, atomic layer deposition (ALD)/CVD is preferred for maximizing the gap-filling window and minimizing the resistance.

Several approaches have been explored for reducing the TaN barrier thickness. First, the minimum thickness can be reduced without sacrificing TaN barrier properties using PVD [9]. In particular, based on time-dependent dielectric breakdown (TDDB) measurements using a planar capacitor structure, TaN barrier characteristics have been shown to be retained even if the thickness is reduced to as low as 0.8 nm. In addition, it has been reported that using a Co/Ru liner instead of a Ta liner significantly improves the overall integrity of the TaN barrier [9]. However, due to the step coverage limit and the overhang problem associated with PVD, it is necessary to switch to ALD as the dimensions decrease. However, TaN thermally deposited using ALD has a higher number of impurities than PVD-fabricated TaN films, a lower film density, a higher resistance, and a lower interface quality, meaning that it cannot emulate the performance of PVD TaN at the same thickness. For this reason, PVD Ta and ALD TaN have been employed as bilayers (1 nm/1 nm) to reduce the thickness while ensuring the barrier properties [10]. Another approach is treating ALD-fabricated TaN in a PVD chamber to transform it into PVD-like film with optimal density and resistivity [11][12]. Using this method, the TaN thickness is 1.2 nm, compared with 1.5 nm for a Co liner and 2.0 nm for a Ru liner [12]. As a result, ALD has been combined with PVD to maintain the barrier properties and a low TaN thickness.

Scaling of the liner has also been actively carried out. The ALD/CVD method is required to overcome the step coverage and overhang problems, but a Ta liner cannot be used. Therefore, replacements for the Ta liner have been considered. Of these, Ru has received significant attention due to its suitability for ALD/CVD and the possibility of direct Cu plating without a PVD Cu seed layer [13][14][15][16][17][18][19]. In addition, Co has also been considered as a replacement for the Ta liner [20]. In [5], a Ru liner was found to be superior to a Co liner for Cu filling and electroplating with a liner thickness of 2 nm. However, the resistance of Ru was about 10% higher than that of Co as revealed by the temperature coefficient of resistance (TCR), which was believed to be due to interface and GB scattering. A Co liner has also been shown to outperform a Ru liner in terms of EM characteristics [21].

However, in order to fully exploit the excellent void-free gap-fill performance of Ru liners, approaches to improving their EM deficiencies have been reported. Co caps have been established as a standard process since the emergence of 14 nm technology. As a result, a significant improvement in EM performance has been observed with a Ru liner as the Co cap thickness increases [21]. It has also been demonstrated that the EM problem arises from the diffusion of Co from the cap to the liner due to the Co concentration gradient between the two [21][22][23]. Thus, a Co-doped Ru liner has been proposed to overcome this problem, and EM improvements have been reported [22][23]. Efforts to scale the TaN barrier and Co/Ru liner continue, but if the metal half-pitch decreases below 10 nm, the barrier/liner scaling limit is reached.

2.2. Selective Barrier Schemes

As advanced technologies emerge, the importance of the resistance and reliability of the vias increases. In particular, via resistance is strongly affected by the bottom thickness of the TaN. Therefore, as scaling progresses, the via resistance rapidly increases due to the thicker TaN. Furthermore, one of the most critical areas of a Cu-based DD structure is the bottom of the via, where the two metal levels meet [24], so selective deposition control of the via bottom barrier is advantageous for improved reliability. In this vein, argon (Ar) sputtering was used as a precleaning PVD barrier/liner [24]. The barrier-first process was conducted in the order of TaN/Ar sputtering/Ta instead of Ar sputtering/TaN/Ta to remove TaN in the via bottom and obtain a Cu/Ta/Cu interface. However, this process disappeared when the precleaning method for removing Cu oxide was changed from Ar sputtering to the oxide-reduction method.

Now that the via size is much smaller, self-assembled monolayers (SAM) have been pursued [25][26]. **Figure 2** presents the process for the formation of a selective barrier on the via bottom. The Cu surface is passivated by depositing a SAM on the Cu surface subjected to the CuO_x reduction treatment. The SAM should be highly selective and self-limited and be adsorbed onto metals but not other peripheral dielectrics. However, when the SAM attaches to the metal surface, it interferes with the adsorption of ALD TaN precursors, resulting in significant nucleation delays in ALD TaN growth [25][26]. As a result, ALD TaN does not deposit on the via bottom area where the SAM is located. The SAM is finally removed. The SAM process needs to be developed further before it can be adopted for mass production. Nevertheless, because it can achieve a reduction in the via resistance of about 50% and its TDDB and EM results are equivalent to the process of record (POR), it is likely to be useful in future advanced technologies [25].

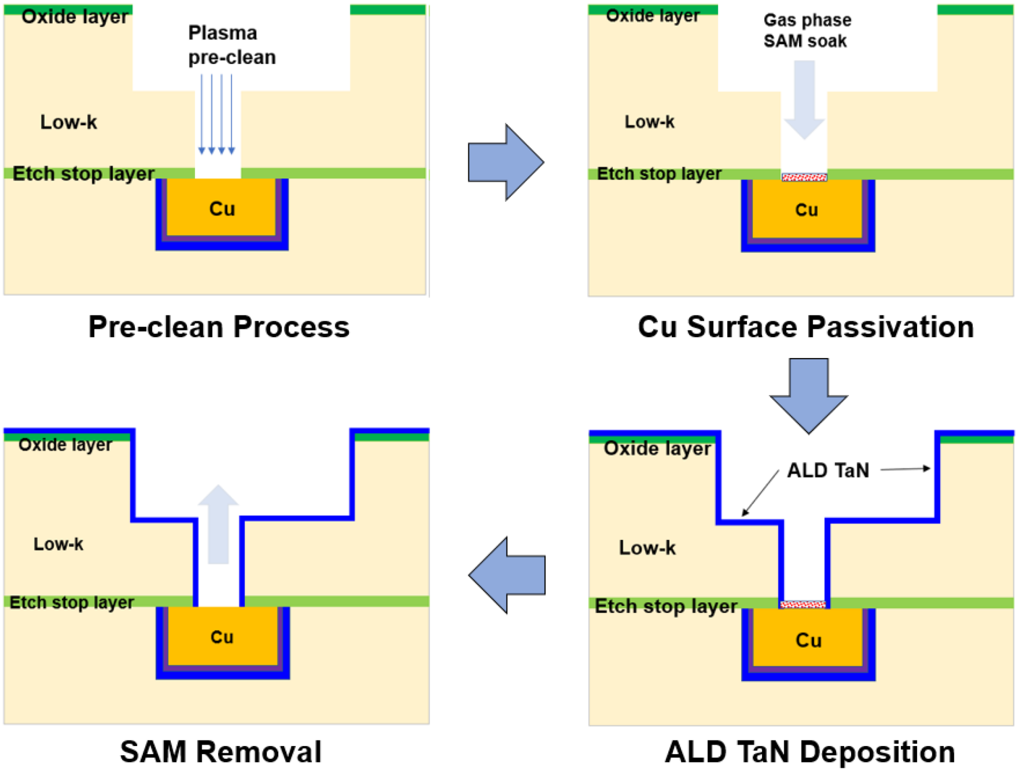
Oxide layer
Plasma pre-clean
Low-k
Etch stop layer
Cu
Pre-clean Process
Oxide layer
Gas phase SAM soak
Low-k
Etch stop layer
Cu
Cu Surface Passivation
Oxide layer
ALD TaN
Low-k
Etch stop layer
Cu
ALD TaN Deposition
Oxide layer
Low-k
Etch stop layer
Cu
SAM Removal

Figure 2. Selective barrier integration process. Reprinted/adapted with permission from Ref. [25]. 2021, IEEE.

2.3. Self-Forming Barriers

Another promising approach to Cu extendibility is the through Co self-forming barrier (tCoSFB), a method in which manganese (Mn) atoms added to the seed Cu diffuse through the thin Co liner layer to form a strong diffusion barrier at the interface between the trench and the dielectric, as seen in **Figure 3** [27][28][29][30].

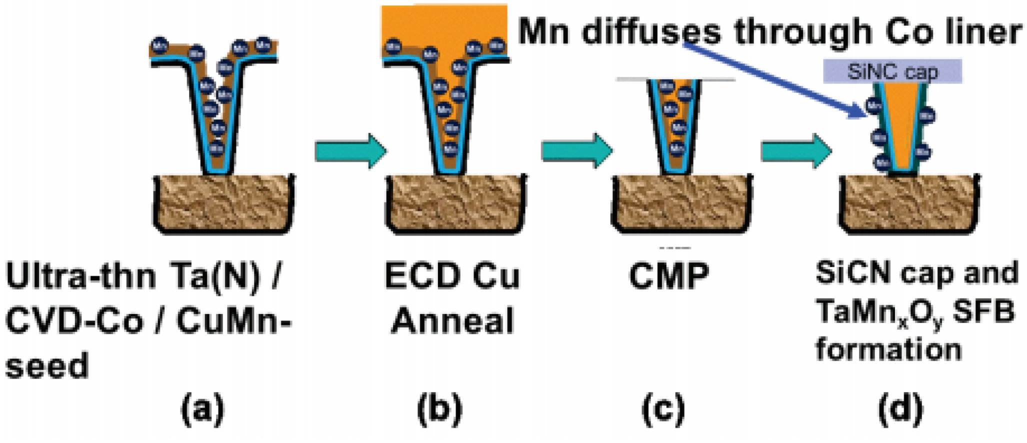
Mn diffuses through Co liner
SiNC cap
Mn
Ultra-thn Ta(N) / CVD-Co / CuMn-seed
(a)
ECD Cu Anneal
(b)
CMP
(c)
SiCN cap and $TaMn_xO_y$ SFB formation
(d)

Figure 3. Through Co self-forming barrier (tCoSFB) structure and fabrication process. (**a**) an ultra-thin Ta(N)/CVD-Co film stack is formed on the patterned ULK pSiCOH surfaces, followed by a high-Mn% PVD-Cu(Mn) seed layer. (**b**) Cu electroplating and post-plating anneal. (**c**) CMP. (**d**) a PECVD SiCN(H) dielectric cap is deposited. Reprinted/adapted with permission from Ref. [27]. 2015, IEEE.

Initially, the Mn dopant is employed to form $MnSi_xO_y$ at the dielectric and Cu interface [28][29][31][32]. If CuMn seed deposition occurs without a barrier/liner and Cu plating and annealing are conducted, an SFB is created. This $MnSi_xO_y$ barrier is very thin and uniform, and its EM and TDDB performance is similar to that of POR. However, vertical trench triangular voltage sweep (VT-TVS) and O_2 barrier tests indicate that $MnSi_xO_y$ is inadequate for blocking Cu and O_2 diffusion, which led to the switch from the SFB to tCoSFB containing thin Ta(N) and Co [33].

The advantage of the tCoSFB process is that the cross-sectional area of Cu in the wiring can be maximized, and low line resistance can be obtained due to the 1 nm thickness of the Co liner and Ta barrier. However, because the line resistance and reliability balance are controlled by the Mn concentration of Cu(Mn) PVD, an increase in resistance may occur. Nevertheless, compared with the POR process, the results are encouraging, with improved resistance and EM and TDDB performance [30][34].

2.4. Hybrid Metallization

At the system-on-chip level, vias have become much more important for signal routing, and via resistance has increased significantly when downscaling the bottom contact area of the via. Therefore, introducing barrierless metal to the via is valuable, and metal−metal selective deposition is essential for the high-aspect-ratio (AR) vias. Hybrid metallization is a method of pre-filling a via with a barrierless metal and then filling the remaining metal area using Cu metallization, as seen in **Figure 4** [35].

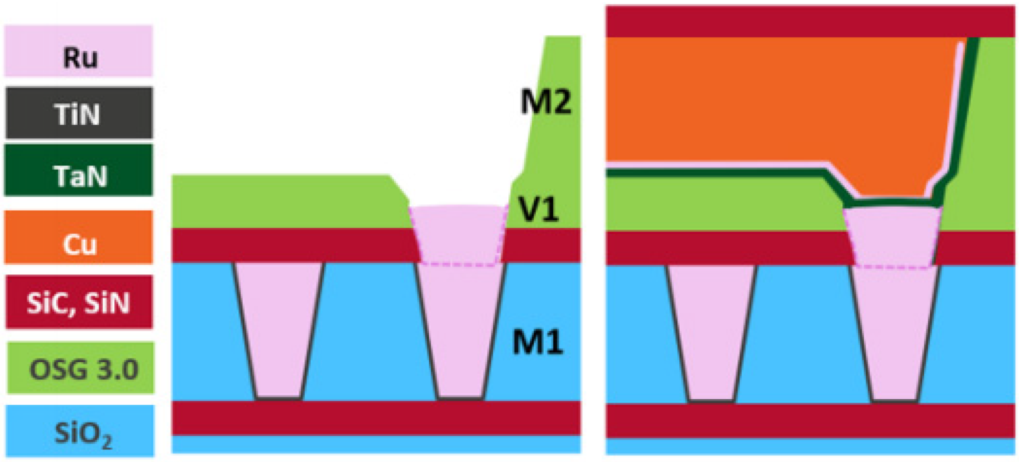

Figure 4. Schematic diagram of Cu hybrid metallization in a two-metal system: (**left**) Ru pre-fill on Ru followed by (**right**) barrier/liner Cu trench metallization. Reprinted/adapted with permission from Ref. [35]. 2020, IEEE.

A barrierless prefill has a number of advantages. First, the prefill moves the barrier position of the Cu DD from the bottom to the top of the via, increasing the tapered via cross-section and reducing the resistance. Second, the gap–fill margin increases because SD trench metallization is employed. Third, because the high-AR vias are excluded, step coverage can be achieved with a thinner barrier/liner [36]. In addition, the optimized barrierless prefilling process may reduce RC delay by increasing the height of the vias and trenches, which can significantly improve circuit performance [37].

The first reported via prefill used Co [37]. However, due to Co ion drift, it was found that barrierless Co was not possible and that TiN barriers are required [36][38]. Ru has been found to be suitable for barrierless prefilling, resulting in a 40% reduction in via resistance and EM results that are similar to those for POR [35].

2.5. Alternative Metals

The thickness of the barrier layer cannot arbitrarily be reduced. If the thickness is less than a certain threshold, it no longer functions as a Cu diffusion barrier. Based on past experimental results, it is unclear whether the barrier/liner combination can have a thickness lower than 2 nm [9][10][11][39]. However, a barrierless solution is required when the half pitch falls below 10 nm, and thus, new metals to replace Cu have been sought. Some of these metals have a larger bulk resistivity than Cu but do not require a thick barrier/liner and exhibit lower resistance at sufficiently small dimensions because their inelastic average free path is shorter than that of Cu (39 nm) [40][41]. Examples of metals and substitutes proposed under these conditions include Ir, Rh, Mo [42], and W [43], but experimentally verified cases are rare except for Co and Ru [44][45][46][47].

Figure 5 displays the line resistance derived from the TCR according to the cross-sectional area of the conductor. Cu has a higher resistance than Ru and Co below ~400 nm^2 at a 16-nm metal width and an AR of 2 [48].

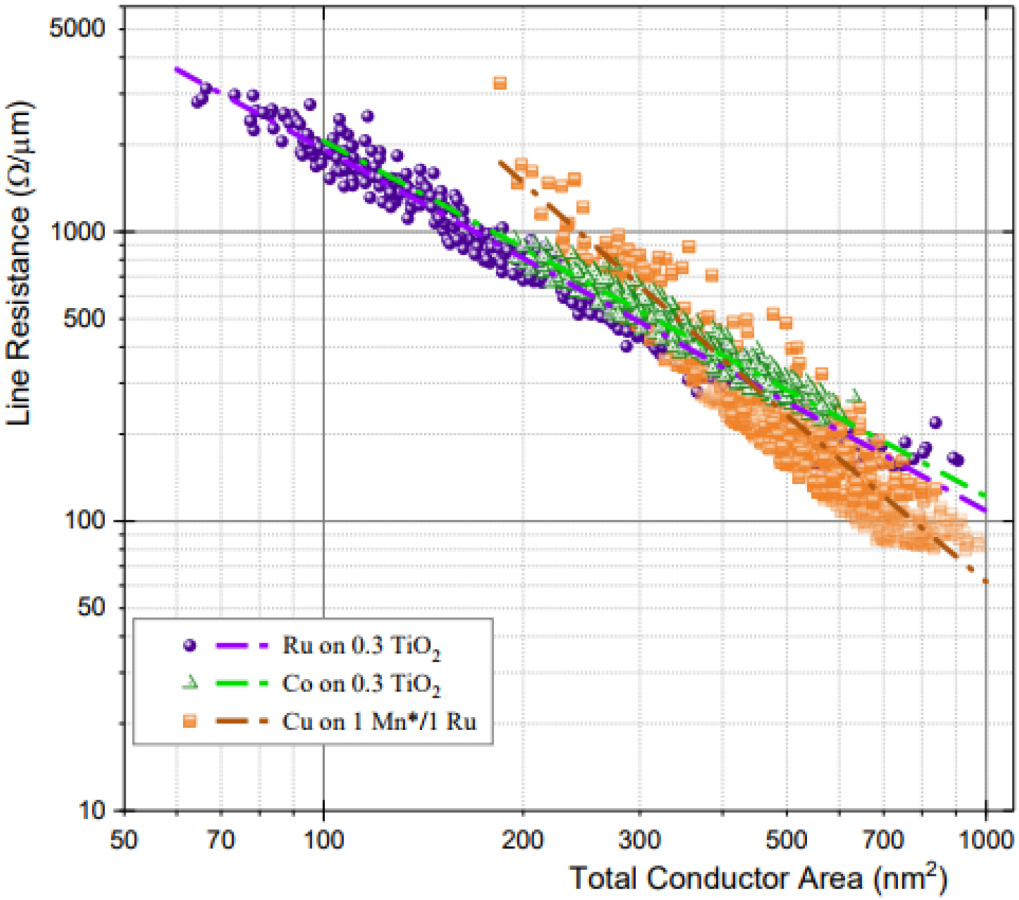

Figure 5. Logarithmic comparison of the damascene line resistance versus the total conductor cross-sectional area for Ru, Co, and Cu nanowires as determined using the TCR. The dotted lines are used to highlight the general trend. Reprinted/adapted with permission from Ref. [48]. 2018, IEEE.

2.6. Ru Semi-Damascene Schemes

Ru can be used in barrierless damascene structures and direct metal etching (DME). **Figure 6** shows Ru metal implemented with subtractive etching.

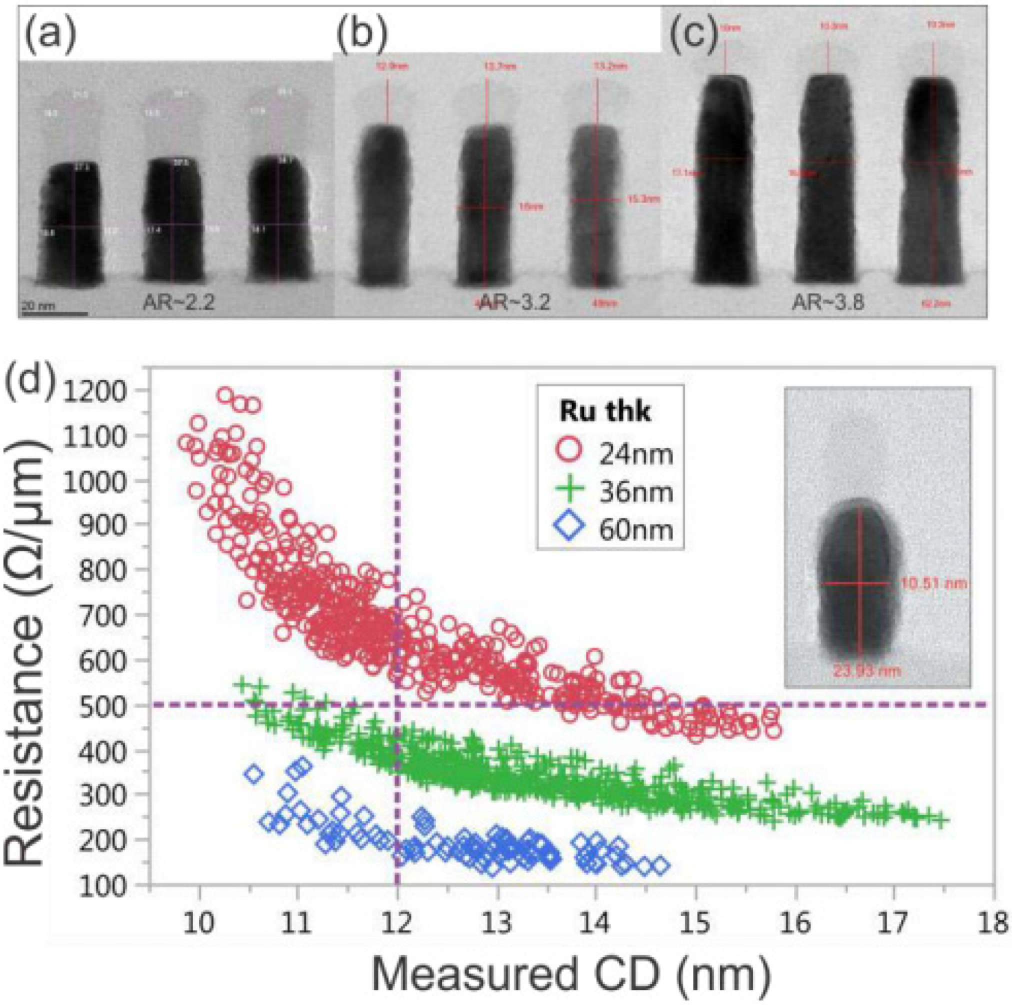

Figure 6. Cross-sectional TEM of patterned Ru films with a thickness of (**a**) 24 nm, (**b**) 36 nm, and (**c**) 60 nm. (**d**) Corresponding R vs. CD for all structures on each wafer. Reprinted/adapted with permission from Ref. [49]. 2018, IEEE.

The use of subtractive etching opens up many possibilities that have not previously been possible for Cu damascene structures. First, because the Ru film is deposited on the entire wafer, the grain size is not limited by the damascene profile width. Therefore, it can significantly restrain the increase in resistance due to GB scattering. Second, the metal thickness is determined by Ru deposition, not by metal CMP. Therefore, if necessary, the resistance can be reduced by increasing the Ru thickness, and there is no AR-related filling problem. Third, because the metal thickness is not affected by the pattern density but is determined by the uniformity of the deposited Ru film, the variation in the metal Rs will be reduced. Finally, a space between Ru metal with an increase in the AR could be introduced by employing an intentional air gap.

The semi-damascene process is an interesting approach that utilizes the advantages of Ru, such as barrierless designs and subtractive etching. This method begins with vias fabricated in a low-k material, and the vias and trench layers are filled using a single deposition step. Subtractive etching is then applied to the trench patterning [49][50][51][52]. According to the latest result, Ru line resistance outperforms Cu at 270 nm^2 or lower (CD < 12 nm) based on line resistance vs. conducting area plot, and the EM and TDDB results are promising so far [53]. For this reason, the Ru semi-damascene process is the most competitive candidate for use in 3 nm technology and lower.

Figure 7 shows the conceptual summary of the metallization approaches mentioned in this section as they have evolved. As shown in the figure, the main trend of metallization has been to reduce the area ratio occupied by the barrier in the scaled wire. Traditional attempts were to reduce the existing barrier/liner (TaN/Ta) thickness by replacing a new process method (ALD) and a new liner material (Co/Ru). After that, it was gradually developed to implement a barrier-free process using Co or Ru. Moreover, the boundary has recently been extended to the subtraction etch process using Ru instead of the Cu damascene scheme.

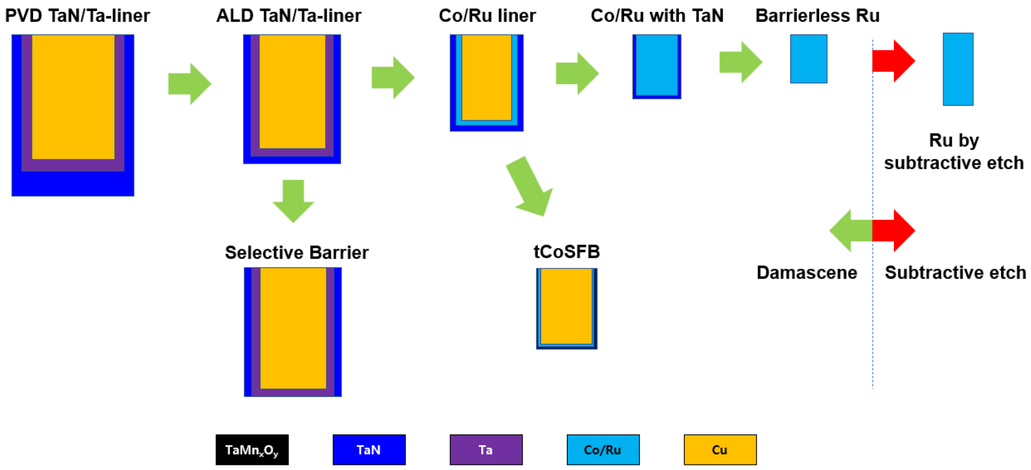

Figure 7. Trends in recent metallization approaches.

In addition to the metallization approaches mentioned here, various studies are being conducted. One of them is the study of a 2D-like barrier. The approach is to minimize the volume fraction of Cu occupied by the barrier by replacing the thick Ta or TaN barrier with 2D-like materials such as graphene [54][55], MoS$_2$ [5][56], TaS$_2$ [5], and WSe$_2$ [5].

In the process of these efforts, the limitation of Cu metallization in CMOS interconnects is becoming more apparent. However, it is interesting that Cu plating is actively applied in other areas, such as solar cells' silicon heterojunction (SHJ) [57][58].

References

1. Davis, J.A.; Venkatesan, R.; Kaloyeros, A.; Beylansky, M.; Souri, S.; Banerjee, K.; Saraswat, K.; Rahman, A.; Reif, R.; Meindl, J. Interconnect limits on gigascale integration (GSI) in the 21st century. Proc. IEEE 2001, 89, 305–324.
2. Bonilla, G.; Lanzillo, N.; Hu, C.-K.; Penny, C.; Kumar, A. Interconnect scaling challenges, and opportunities to enable system-level performance beyond 30 nm pitch. In Proceedings of the 2020 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 12–18 December 2020.
3. Theis, T.N. The future of interconnection technology. IBM J. Res. Dev. 2000, 44, 379–390.
4. Havemann, R.; Hutchby, J. High-performance interconnects: An integration overview. Proc. IEEE 2001, 89, 586–601.
5. Lo, C.-L.; Helfrecht, B.A.; He, Y.; Guzman, D.M.; Onofrio, N.; Zhang, S.; Weinstein, D.; Strachan, A.; Chen, Z. Opportunities and challenges of 2D materials in back-end-of-line interconnect scaling. J. Appl. Phys. 2020, 128, 080903.
6. Chang, S.Y.; Wan, C.C.; Wang, Y.Y. Selectivity enhancement of electroless Co deposition for Cu capping process via spontaneous diazonium ion reduction. Electrochem. Solid-State Lett. 2007, 10, D43.
7. Shimada, M.; Moriyama, M.; Ito, K.; Tsukimoto, S.; Murakami, M. Electrical resistivity of polycrystalline Cu interconnects with nano-scale linewidth. J. Vac. Sci. Technol. B Microelectron. Nanometer Struct. Process. Meas. Phenom. 2006, 24, 190–194.
8. Steinhögl, W.; Schindler, G.; Steinlesberger, G.; Engelhardt, M. Size-dependent resistivity of metallic wires in the mesoscopic range. Phys. Rev. B 2002, 66, 075414.
9. Witt, C.; Yeap, K.; Lesniewska, A.; Wan, D.; Jordan, N.; Ciofi, I.; Wu, C.; Tokei, Z. Testing the limits of TaN barrier scaling. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.
10. Motoyama, K.; van der Straten, O.; Maniscalco, J.; Huang, H.; Kim, Y.; Choi, J.; Lee, J.; Hu, C.-K.; McLaughlin, P.; Standaert, T.; et al. Ru liner scaling with ALD TaN barrier process for low resistance 7 nm Cu interconnects and beyond. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.
11. Wu, Z.; Li, R.; Xie, X.; Suen, W.; Tseng, J.; Bekiaris, N.; Vinnakota, R.; Kashefizadeh, K.; Naik, M. PVD-treated ALD TaN for Cu interconnect extension to 5 nm node and beyond. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.

12. Bhosale, P.S.; Maniscalco, J.; Lanzillo, N.; Nogami, T.; Canaperi, D.; Motoyama, K.; Huang, H.; McLaughlin, P.; Shaviv, R.; Stolfi, M.; et al. Modified ALD TaN barrier with Ru liner and dynamic Cu reflow for 36nm pitch interconnect integration. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.

13. Yang, C.-C.; Spooner, T.; Ponoth, S.; Chanda, K.; Simon, A.; Lavoie, C.; Lane, M.; Hu, C.-K.; Liniger, E.; Gignac, L.; et al. Physical, electrical, and reliability characterization of Ru for Cu interconnects. In Proceedings of the 2006 International Interconnect Technology Conference, Burlingame, CA, USA, 5–7 June 2006.

14. Abe, M.; Ueki, M.; Tada, M.; Onodera, T.; Furutake, N.; Shimura, K.; Saito, S.; Hayashi, Y. Highly-oriented PVD ruthenium liner for low-resistance direct-plated Cu interconnects. In Proceedings of the 2007 IEEE International Interconnect Technology Conference, Burlingame, CA, USA, 4–6 June 2007.

15. Mori, K.; Ohmori, K.; Torazawa, N.; Hirao, S.; Kaneyama, S.; Korogi, H.; Maekawa, K.; Fukui, S.; Tomita, K.; Inoue, M.; et al. Effects of Ru-Ta alloy barrier on Cu filling and reliability for Cu interconnects. In Proceedings of the 2008 International Interconnect Technology Conference, Burlingame, CA, USA, 1–4 June 2008.

16. Huang, H.Y.; Hsieh, C.H.; Jeng, S.M.; Tao, H.J.; Cao, M.; Mii, Y.J. A new enhancement layer to improve copper interconnect performance. In Proceedings of the 2010 IEEE International Interconnect Technology Conference, Burlingame, CA, USA, 6–9 June 2010.

17. Rullan, J.; Ishizaka, T.; Cerio, F.; Mizuno, S.; Mizusawa, Y.; Ponnuswamy, T.; Reid, J.; McKerrow, A.; Yang, C.-C. Low resistance wiring and 2Xnm void free fill with CVD Ruthenium liner and DirectSeed TM copper. In Proceedings of the 2010 IEEE International Interconnect Technology Conference, Burlingame, CA, USA, 6–9 June 2010.

18. Yang, C.-C.; Cohen, S.; Shaw, T.; Wang, P.-C.; Nogami, T.; Edelstein, D. Characterization of “Ultrathin-Cu”/Ru (Ta)/TaN liner stack for copper interconnects. IEEE Electron Device Lett. 2010, 31, 722–724.

19. Swerts, J.; Armini, S.; Carbonell, L.; Delabie, A.; Franquet, A.; Mertens, S.; Popovici, M.; Schaekers, M.; Witters, T.; Tökei, Z.; et al. Scalability of plasma enhanced atomic layer deposited ruthenium films for interconnect applications. J. Vac. Sci. Technol. A Vac. Surf. Film. 2012, 30, 01A103.

20. He, M.; Zhang, X.; Nogami, T.; Lin, X.; Kelly, J.; Kim, H.; Spooner, T.; Edelstein, D.; Zhao, L. Mechanism of Co liner as enhancement layer for Cu interconnect gap-fill. J. Electrochem. Soc. 2013, 160, D3040.

21. Wu, Z.; Chen, F.; Shen, G.; Hu, Y.; Pethe, S.; Lee, J.J.; Tseng, J.; Suen, W.; Vinnakota, R.; Kashefizadeh, K.; et al. Pathfinding of Ru-Liner/Cu-Reflow Interconnect Reliability Solution. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.

22. Motoyama, K.; van der Straten, O.; Maniscalco, J.; Cheng, K.; DeVries, S.; Huang, H.; Shen, T.; Lanzillo, N.; Hosadurga, S.; Park, K.; et al. Co-doped Ru liners for highly reliable Cu interconnects with selective Co cap. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–8 October 2020.

23. Motoyama, K. EM performance improvements for Cu interconnects with Ru-based liner and Co cap in advanced nodes. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021.

24. Alers, G.; Rozbicki, R.T.; Harm, G.J.; Kailasam, S.; Ray, G.W.; Danek, M. Barrier-first integration for improved reliability in copper dual damascene interconnects. In Proceedings of the IEEE 2003 International Interconnect Technology Conference (Cat. No. 03TH8695), Burlingame, CA, USA, 4 June 2003.

25. You, S.; Ren, H.; Naik, M.; Chen, L.; Chen, F.; Cervantes, C.L.; Xie, X.; Kashefizadeh, K. Selective Barrier for Cu Interconnect Extension in 3nm Node and Beyond. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021.

26. Kawasaki, H.; Iwashita, M.; Warashina, H.; Nagai, H.; Iwai, K.; Komatsu, H.; Ozaki, Y.; Pattanaik, G. Advanced Damascene integration using selective deposition of barrier metal with Self Assemble Monolayer. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021.

27. Nogami, T.; Briggs, B.D.; Korkmaz, S.; Chae, M.; Penny, C.; Li, J.; Wang, W.; McLaughlin, P.S.; Kane, T.; Parks, C.; et al. Through-Cobalt Self Forming Barrier (tCoSFB) for Cu/ULK BEOL: A novel concept for advanced technology nodes. In Proceedings of the 2015 IEEE International Electron Devices Meeting (IEDM), Washington, DC, USA, 7–9 December 2015.

28. Koike, J.; Haneda, M.; Iijima, J.; Wada, M. Cu alloy metallization for self-forming barrier process. In Proceedings of the 2006 International Interconnect Technology Conference, Burlingame, CA, USA, 5–7 June 2006.

29. Siew, Y.K.; Jourdan, N.; Ciofi, I.; Croes, K.; Wilson, C.J.; Tang, B.J.; Demuynck, S.; Wu, Z.; Ai, H.; Cellier, D.; et al. Cu wire resistance improvement using mn-based self-formed barriers. In Proceedings of the IEEE International Interconnect Technology Conference, San Jose, CA, USA, 20–23 May 2014.

30. Nogami, T.; Zhang, X.; Kelly, J.; Briggs, B.; You, H.; Patlolla, R.; Huang, H.; McLaughlin, P.; Lee, J.; Shobha, H.; et al. Comparison of key fine-line BEOL metallization schemes for beyond 7 nm node. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017.

31. Usui, T.; Nasu, H.; Koike, J.; Wada, M.; Takahashi, S.; Shimizu, N.; Nishikawa, T.; Yoshimaru, A.; Shibata, H. Low resistive and highly reliable Cu dual-damascene interconnect technology using self-formed MnSi/sub x/O/sub y/barrier layer. In Proceedings of the IEEE 2005 International Interconnect Technology Conference, Burlingame, CA, USA, 6–8 June 2005.

32. Usui, T.; Tsumura, K.; Nasu, H.; Hayashi, Y.; Minamihaba, G.; Toyoda, H.; Sawada, H.; Ito, S.; Miyajima, H.; Watanabe, K.; et al. High performance ultra low-k (k = 2.0/keff = 2.4)/Cu dual-damascene interconnect technology with self-formed MnSixOy barrier layer for 32 nm-node. In Proceedings of the 2006 International Interconnect Technology Conference, Burlingame, CA, USA, 5–7 June 2006.

33. Nogami, T.; Chae, M.; Penny, C.; Shaw, T.; Shobha, H.; Li, J.; Cohen, S.; Hu, C.-K.; Zhang, X.; He, M.; et al. Performance of ultrathin alternative diffusion barrier metals for next-Generation BEOL technologies, and their effects on reliability. In Proceedings of the IEEE International Interconnect Technology Conference., San Jose, CA, USA, 20–23 May 2014.

34. Nogami, T.; Huang, H.; Shobha, H.; Patlolla, R.; Kelly, J.; Penny, C.; Hu, C.-K.; Sil, D.; Devries, S.; Lee, J.; et al. Technology challenges and enablers to extend Cu metallization to beyond 7 nm node. In Proceedings of the 2019 Symposium on VLSI Technology, Kyoto, Japan, 9–14 June 2019.

35. van der Veen, M.H.; Soethoudt, J.; Delabie, A.; Pedreira, O.V.; Gonzalez, V.V.; Lariviere, S.; Teugels, L.; Jourdan, N.; Decoster, S.; Struyf, H.; et al. Hybrid Metallization with Cu in sub 30nm Interconnects. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–8 October 2020.

36. van der Veen, M.H.; Vandersmissen, K.; Dictus, D.; Demuynck, S.; Liu, R.; Bin, X.; Nalla, P.; Lesniewska, A.; Hall, L.; Croes, K.; et al. Cobalt bottom-up contact and via prefill enabling advanced logic and DRAM technologies. In Proceedings of the 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015.

37. Zheng, J.-F.; Chen, P.; Baum, T.H.; Lieten, R.R.; Hunks, W.; Lippy, S.; Frye, A.; Li, W.; O'Neill, J.; Xu, J.; et al. Selective Co growth on Cu for void-free via fill. In Proceedings of the 2015 IEEE International Interconnect Technology Conference and 2015 IEEE Materials for Advanced Metallization Conference (IITC/MAM), Grenoble, France, 18–21 May 2015.

38. Steinhögl, W.; Schindler, G.; Steinlesberger, G.; Traving, M.; Engelhardt, M. Comprehensive study of the resistivity of copper wires with lateral dimensions of 100 nm and smaller. J. Appl. Phys. 2005, 97, 023706.

39. Lanzillo, N.A.; Yang, C.-C.; Motoyama, K.; Huang, H.; Cheng, K.; Maniscalco, J.; Van Der Straten, O.; Penny, C.; Standaert, T.; Choi, K. Exploring the limits of cobalt liner thickness in advanced copper interconnects. IEEE Electron Device Lett. 2019, 40, 1804–1807.

40. Hu, C.-K.; Kelly, J.; Chen, J.H.-C.; Huang, H.; Ostrovski, Y.; Patlolla, R.; Peethala, B.; Adusumilli, P.; Spooner, T.; Gignac, L.M.; et al. Electromigration and resistivity in on-chip Cu, Co and Ru damascene nanowires. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017; pp. 1–3.

41. Bekiaris, N.; Wu, Z.; Ren, H.; Naik, M.; Park, J.H.; Lee, M.; Ha, T.H.; Hou, W.; Bakke, J.R.; Gage, M.; et al. Cobalt fill for advanced interconnects. In Proceedings of the 2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017.

42. Tierno, D.; Hosseini, M.; van der Veen, M.; Dangol, A.; Croes, K.; Demuynck, S.; Tokei, Z.; Litta, E.; Horiguchi, N. Reliability of Barrierless PVD Mo. In Proceedings of the 2021 IEEE International Interconnect Technology Conference (IITC), Kyoto, Japan, 6–9 July 2021.

43. Choi, D.; Barmak, K. On the potential of tungsten as next-generation semiconductor interconnects. Electron. Mater. Lett. 2017, 13, 449–456.

44. Wen, L.G.; Roussel, P.; Pedreira, O.V.; Briggs, B.; Groven, B.; Dutta, S.; Popovici, M.I.; Heylen, N.; Ciofi, I.; Vanstreels, K.; et al. Atomic layer deposition of ruthenium with TiN interface for sub-10 nm advanced interconnects beyond copper. ACS Appl. Mater. Interfaces 2016, 8, 26119–26125.

45. Zhang, X.; Huang, H.; Patlolla, R.; Wang, W.; Mont, F.W.; Li, J.; Hu, C.-K.; Liniger, E.G.; McLaughlin, P.S.; Labelle, C.; et al. Ruthenium interconnect resistivity and reliability at 48 nm pitch. In Proceedings of the 2016 IEEE International Interconnect Technology Conference/Advanced Metallization Conference (IITC/AMC). San Jose, CA, USA, 23–26 May 2016.

46. Nogami, T.; Patlolla, R.; Kelly, J.; Briggs, B.; Huang, H.; Demarest, J.; Li, J.; Hengstebeck, R.; Zhang, X.; Lian, G.; et al. Cobalt/copper composite interconnects for line resistance reduction in both fine and wide lines. In Proceedings of the

2017 IEEE International Interconnect Technology Conference (IITC), Hsinchu, Taiwan, 16–18 May 2017.

47. Dutta, S.; Kundu, S.; Gupta, A.; Jamieson, G.; Granados, J.F.G.; Bommels, J.; Wilson, C.J.; Tokei, Z.; Adelmann, C. Highly scaled ruthenium interconnects. IEEE Electron Device Lett. 2017, 38, 949–951.
48. van der Veen, M.H.; Heyler, N.; Pedreira, O.V.; Ciofi, I.; Decoster, S.; Gonzalez, V.V.; Jourdan, N.; Struyf, H.; Croes, K.; Wilson, C.J.; et al. Damascene benchmark of Ru, Co and Cu in scaled dimensions. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.
49. Wan, D.; Paolillo, S.; Rassoul, N.; Kotowska, B.K.; Blanco, V.; Adelmann, C.; Lazzarino, F.; Ercken, M.; Murdoch, G.; Bommels, J.; et al. Subtractive etch of ruthenium for sub-5nm interconnect. In Proceedings of the 2018 IEEE International Interconnect Technology Conference (IITC), Santa Clara, CA, USA, 4–7 June 2018.
50. Croes, K.; Adelmann, C.; Wilson, C.J.; Zahedmanesh, H.; Pedreira, O.V.; Wu, C.; Leśniewska, A.; Oprins, H.; Beyne, S.; Ciofi, I.; et al. Interconnect metals beyond copper: Reliability challenges and opportunities. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018.
51. Murdoch, G.; Tokei, Z.; Paolillo, S.; Pedreira, O.V.; Vanstreels, K.; Wilson, C.J. Semidamascene Interconnects for 2nm node and Beyond. In Proceedings of the 2020 IEEE International Interconnect Technology Conference (IITC), San Jose, CA, USA, 5–8 October 2020.
52. Lesniewska, A.; Roussel, P.; Tierno, D.; Gonzalez, V.V.; van der Veen, M.H.; Verdonck, P.; Jourdan, N.; Wilson, C.; Tokei, Z.; Croes, K. Dielectric reliability study of 21 nm pitch interconnects with barrierless Ru fill. In Proceedings of the 2020 IEEE International Reliability Physics Symposium (IRPS), Dallas, TX, USA, 28 April–30 May 2020.
53. Murdoch, G.; O'Toole, M.; Marti, G.; Pokhrel, A.; Tsvetanova, D.; Decoster, S.; Kundu, S.; Oniki, Y.; Thiam, A.; Le, Q.; et al. First demonstration of Two Metal Level Semi-damascene Interconnects with Fully Self-aligned Vias at 18MP. In Proceedings of the 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 13–17 June 2022.
54. Son, M.; Jang, J.; Lee, Y.; Nam, J.; Hwang, J.Y.; Kim, I.S.; Lee, B.H.; Ham, M.-H.; Chee, S.-S. Copper-graphene heterostructure for back-end-of-line compatible high-performance interconnects. NPJ 2D Mater. Appl. 2021, 5, 41.
55. Nogami, T.; Nguyen, S.; Huang, H.; Lanzillo, N.; Shobha, H.; Li, J.; Peethela, B.; Parbatani, A.; van Schravendijk, B.; Varadarajan, B.; et al. Electromigration and line R of graphene capped Cu dual Damascene interconnect. In Proceedings of the 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 11–16 December 2021.
56. Lo, C.-L.; Zhang, K.; Smith, R.S.; Shah, K.; Robinson, J.A.; Chen, Z. Large-area, single-layer molybdenum disulfide synthesized at BEOL compatible temperature as Cu diffusion barrier. IEEE Electron Device Lett. 2018, 39, 873–876.
57. Yu, J.; Li, J.; Zhao, Y.; Lambertz, A.; Chen, T.; Duan, W.; Liu, W.; Yang, X.; Huang, Y.; Ding, K. Copper metallization of electrodes for silicon heterojunction solar cells: Process, reliability and challenges. Sol. Energy Mater. Sol. Cells 2021, 224, 110993.
58. Yang, L.; Zhong, S.; Zhang, W.; Li, X.; Li, Z.; Zhuang, Y.; Wang, X.; Zhao, L.; Cao, X.; Deng, X.; et al. Study and development of rear-emitter Si heterojunction solar cells and application of direct copper metallization. Prog. Photovolt. Res. Appl. 2018, 26, 385–396.

Retrieved from https://encyclopedia.pub/entry/history/show/67586