

III-V Semiconductor Nanowire Ordered Arrays

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Contributor: Francesco Rossella

Ordered arrays of vertically aligned semiconductor nanowires are regarded as promising candidates for the realization of all-dielectric metamaterials, artificial electromagnetic materials, whose properties can be engineered to enable new functions and enhanced device performances with respect to naturally existing materials. In this review we account for the recent progresses in substrate nanopatterning methods, strategies and approaches that overall constitute the preliminary step towards the bottom-up growth of arrays of vertically aligned semiconductor nanowires with a controlled location, size and morphology of each nanowire. While we focus specifically on III-V semiconductor nanowires, several concepts, mechanisms and conclusions reported in the manuscript can be invoked and are valid also for different nanowire materials.

Keywords: semiconductor nanowire ordered arrays ; substrate patterning ; nanowire metasurfaces

1. Introduction

Semiconductor nanowires have emerged as a powerful class of materials with great potential for applications in many fields of technology, due to their outstanding electronic and optical properties and a relatively easy, controllable and scalable bottom-up growth process ^{[1][2]}. Their employment at large scale sets challenging requirements in terms of position, size and shape control of the individual nano-objects in nanowire ensembles ^{[3][4]}. This level of control represents a necessary step towards the realization of reliable and reproducible devices exploiting a very large number of nanowires for their operation, and for the integration of nanowire-based systems and devices with other technological platforms, such as silicon electronics and photonics ^{[5][6]}. Ordered arrays of vertically aligned semiconductor nanowires (NWs) have gained significant attention over the last two decades, as they have emerged as promising platforms in several fields of research including optics ^{[7][8][9]}, electronics ^{[10][11][12]}, energy ^{[13][14][15][16]}, quantum computing ^{[17][18]}, integrated photonics ^{[19][20]}, sensing ^{[21][22][23]}, and life sciences ^{[24][25]}.

By exploiting the advances in nanofabrication and growth techniques, nanowire assemblies can nowadays be finely designed in order to fully tune and adjust their physical properties ^[26]. In particular, nanowire arrays can be engineered to realize nanowire metamaterials and metasurfaces, artificially prepared electromagnetic materials made of resonant subwavelength structures, showing effective medium properties that do not exist in nature. Photonic metamaterials made of assemblies of metal or semiconductor NWs have been experimentally and theoretically investigated ^{[27][28]}; nanowire metamaterials with optical negative refraction ^[29], optical cloaks ^[30], electrically tunable metamaterials ^[31], and near zero reflectance materials ^[32] have been reported.

As shown in the following sections, nanowires are available in a large variety of materials and they can incorporate heterostructures made of different components, even combining materials that are challenging to be combined in their thin film counterparts.

In this review we shine light on the recent progresses in the bottom-up realization of ordered arrays of vertically arranged semiconductor nanowires and nanowire metasurfaces by systematically reviewing the role of substrate pre-patterning, the current opportunities and the experimental limitations. Indeed, the realization of highly ordered nanowire arrays requires a preliminary step of substrate lithographic patterning, aimed at defining the specific nanowire locations on the substrate. Notably, the geometry and quality of the pattern employed to assist the nanowire growth dramatically affects the characteristics of the grown nanowire array. This study pinpoints and fixes the key concepts and phenomena guiding the subtle interdependence between surface pre-patterning and nanowire array growth. Such concepts and phenomena are typically common to several nanowire materials and growth approaches. In our study we devote particular attention to nanowire systems made of III-V semiconductor compounds; however, several mechanisms discussed for III-V's can be invoked with minor differences for other semiconductors and semiconductor compounds.

2. Semiconductor Nanowires and Nanowire Arrays

A fundamental boost in nanowire research originated from the pioneering works of Lieber, Yang and Samuelson in the '90s, who were the first to demonstrate the possibility to realize, by using bottom-up self-assembling growth techniques, very high quality nanowires structures [33][34][35][36], thus sparking the interest of the scientific community in this field. In particular, they demonstrated the versatility of the bottom-up growth in enabling the realization, during growth, of very high quality nanowire crystals and heterostructures, made of combinations of different materials, resulting in very abrupt and atomically sharp interfaces. This opportunity is permitted by the strain relaxation along the nanowire sidewalls occurring in bottom-up growth, enabling the coupling of materials with a high lattice constant mismatch, such as, for example, III-V materials on silicon substrates [1][37][38]. Moreover, self assembling generally enables the realization of less defected surfaces and a better control of the resulting facets [1] with respect to top-down lithography approaches. These advantages made bottom-up self-assembling the most eligible approach for nanowire growth.

In recent years, new avenues for exploration in the nanowire field have been enabled by the advances in growth and nanofabrication techniques, which has allowed the design of engineered nanowire patterns with a fine control over the size, shape, material composition, location, and orientation of each individual nanowire.

Apart from the interest related to the exploration of new physical phenomena, such as advanced mechanisms of light propagation control at the nanoscale, the deterministic growth at selected locations on the substrate of nanowires represents the fundamental challenge to be addressed from the perspective of the full exploitation of nanowire potentialities in large scale applications, possibly with their integration with more mature (e.g., silicon-based) technological platforms [3][4].

With rare exceptions [39], most of the processes for the fabrication of ordered arrays of vertical nanowires, especially when high quality and high pattern precision is required, include at least one stage of lithographic patterning as the fundamental step to define the pattern geometry. As a matter of fact, the final outcome—the nanowire array—is dramatically affected not only by the specific growth parameters ruling the kinetics and thermodynamics of the growth mechanisms, but also by the geometry and quality of the pattern employed to assist the nanowire growth [3][40][41]. This is the reason why, in the context of ordered nanowire array realization, the role of the substrate patterning deserves a dedicated and accurate investigation: reviewing the investigation efforts spent by the scientific community in this direction is actually the goal of the present work.

3. Bottom-Up Approaches to the Realization of Ordered Arrays of Vertically Aligned Semiconductor Nanowires

The bottom-up approaches for the realization of ordered arrays of semiconductor nanowires mainly rely on two prominent techniques: nanoparticle-assisted growth, which is at present the most commonly used technique for NW growth [5][37][42], and catalyst-free growth, often obtained by selective area epitaxy. Both these techniques enable nanowires growth at specific locations predefined by lithographic pre patterning of the substrate.

The choice of the lithographic patterning technique for substrate preparation depends on the desired specifications of the array. The nanowires composing an engineered array can be individually seeded, or grown randomly on selected areas. In the latter case, for growth areas with a feature size above several hundreds of nanometers, or even micrometers, the catalyst pattern can simply be defined by resorting to micropatterning techniques (e.g., UV lithography or laser writing) and then the nanowire growth can be obtained by applying the same processes commonly employed for NW VLS growth on unpatterned substrates, e.g., thin metal layer deposition followed by thermal de-wetting or a standard deposition of metal colloidal nanoparticles [43]. However, studies on the role of the catalyst's shape in an individually seeded nanowire suggest that for growth areas below a few hundreds of nanometers, a dedicated optimization of the growth parameters is definitively required [44] (See Section 3.1).

The most common technique exploited for the definition of precisely located metal seeds for ordered nanowire array realization is electron beam lithography (EBL) [45][46][47][44][48].

In **Figure 1** some examples of InAs nanowire-ordered arrays grown on a prepatterned substrate realized by electron beam lithography are shown [49].

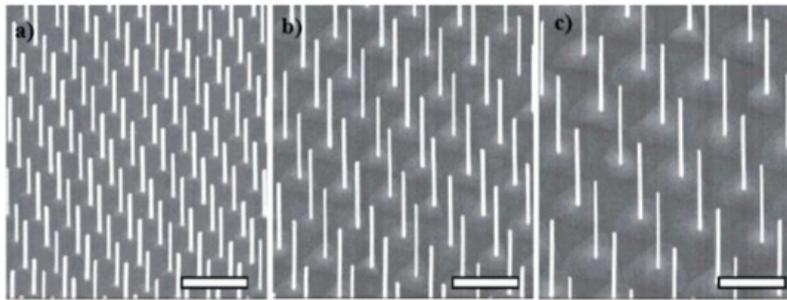


Figure 1. SEM tilted views of nanowire InAs NW arrays grown from EBLprepatterned substrates. The NWs have same diameters but different inter-wire distances: (a) 0.5 μm , (b) 0.75 μm and (c) 1 μm . The nanowires were grown from Au catalysts realized by electron beam lithography. Scale bar is 1 μm in each panel. (Reprinted with permission of Ref. [49]).

4. Influence of the Pattern Characteristics

The study of the role of the pattern characteristics, namely the metal seed size and the aspect ratio in metal-catalyzed growth, the hole sizes and aspect ratio in template assisted growth and the pitch, in enabling the reliable fabrication of uniform and controlled nanowire arrays, is sparsely addressed in the literature, but its crucial impact is fully recognized [3][40][44]. Some relevant information about the main mechanisms relating the pattern characteristics to the final array properties, as well as the connected experimental limitations in fabrication, can anyhow be gathered from the abundant literature in the growth field, which also includes some interesting recent papers and reviews [1][5]. Trying to put forward a comprehensive discussion including all the reported results, obtained for a large variety of nanowire materials, growth techniques and conditions, would be a very hard task, because the reported findings are most of the time dependent on the specific used growth conditions, adding a further complexity to the analysis.

For the growth conditions at which only axial growth occurs, the nanowire diameter is defined by the geometric parameters of the individual element in the pre-patterned substrate. As previously mentioned the current substrate patterning techniques allow to define the catalyst seeds and etching mask openings in the scale of a few nm diameter. However, the patterning technology resolution can be assumed only as a rough estimation of the lower NW diameter and array pitch, as the individual pattern featured size often does not correspond precisely to the nanowire size [5]. In VLS nanowire growth of III-V semiconductor compounds and other semiconductor materials, the nanowire diameter depends in first approximation on the seed particle volume, which includes both the starting catalyst droplet volume and the amount of the source materials incorporated into the seed [8][45]. Detailed models to explain the mechanism have been proposed [50][51]. During the initial stages of the growth, the catalyst nanoparticles will melt and often expand as they become saturated with the source materials, causing the nanowire diameter to exceed the initial catalyst particle size of several nanometers [44][52]. The contact angle formed by the metal catalyst and the nanowire growth facet, which is correlated to the catalyst stability at the nanowire tip, also plays a crucial role [5], affecting the diameter [9][53] and in some cases also the crystal structure [54], and growth direction [55]. Similarly, in selective area growth, the nanowire diameters are defined by the dimension of the openings in the growth mask. Moreover, in this case, the smallest diameter obtained for self-catalyzed growth is around 10 nm, which was obtained with an accurate control of the contact angle. In general, reaching nanowire diameters in the sub-30 nm range by bottom-up growth—which would enable quantum confinement functionalities—is presently considered a challenging task, and the possibility to realize large area arrays of controlled nanowires in that scale range still needs optimization [5][56][57]. Moreover, changes in diameter along the NW body (tapering and radial vapor-solid growth) and local random or non-random fluctuations of the diameter are often observed.

An alternative method to obtain a very high yield in catalyst-assisted growth is to adopt a combined approach, which exploits selective area growth, combined with a catalyst-assisted method [58].

Notably, the optimal control of the individual element geometry of the pattern is not sufficient to guarantee a very high yield in the final NW array: several other growth parameters need to be optimized, as will be briefly discussed in the sections that follow.

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