ATtiny Microcontroller Comparison Chart

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ATtiny (also known as TinyAVR) are a subfamily of the popular 8-bit AVR microcontrollers, which typically has fewer features, fewer I/O pins, and less memory than other AVR series chips. The first members of this family were released in 1999 by Atmel (later acquired by Microchip Technology in 2016).

Keywords: microcontrollers ; atmel ; tinyavr

1. Features

ATtiny microcontrollers specifically excludes various common features, such as: USB peripheral, DMA controller, crypto engine, or an external memory bus.

The following table summarizes common features of the ATtiny microcontrollers, for easy comparison. This table is not meant to be an unabridged feature list.

Device (family)[1]	Max clock (MHz)	Flash (KiB)	SRAM (bytes)	EEPROM (bytes)	UART	I²C (TWI (Two-wire interface))	SPI	Timers 8/12/16 (bits)	PWM (Pulse-width modulated) [2]	ADC pins	GPIO pins	IC Packages	GCC arch ID [3][4]	Pgm Dbg	Refs
ATtiny11, ATtiny11L	6, 2	1	No	No	No	No	No	1 / 0 / 0	No	No	5	DIP-8N, SO200-8	avr1	HVSP	[5]
ATtiny12, ATtiny12L, ATtiny12V	8, 1.2	1	No	64	No	No	No	1 / 0 / 0	No	No	5	DIP-8N, SO200-8	avr1	ISP, HVSP	[5]
ATtiny15L	1.6	1	No	64	No	No	No	2 / 0 / 0	yes	4	6	DIP-8N, SO200-8	avr1	ISP, HVSP	[6]
ATtiny28L, ATtiny28V	4, 1.2	2	No	No	No	No	No	1 / 0 / 0	1 x 1	No	11	DIP-28N, TQFP-32, QFN-32	avr1	HVPP	[7]
ATtiny22, ATtiny22L	8, 4	2	128	128	No	No	No	1 / 0 / 0	No	No	5	DIP-8N, SO200-8	avr2	ISP, HVSP	[8]
ATtiny26, ATtiny26L	16, 8	2	128	128	USI*	master, slave*	master, slave*	2 / 0 / 0	1 x 2	11	16	DIP-20N, SO300-20, QFN-32	avr2	ISP, HVPP	[9]
ATtiny13, ATtiny13V, ATtiny13A	20, 10	1	64	64	No	No	No	1 / 0 / 0	1 x 2	4	6	DIP-8N, SO150-8, SO209-8, VQFN-10, WQFN-20	avr2.5	ISP, dW, HVSP	[10] [11] [12]
ATtiny24, ATtiny24V, ATtiny24A, ATtiny44, ATtiny44V, ATtiny44A, ATtiny84, ATtiny84V, ATtiny84A	20, 10	2, 4, 8	128, 256, 512	128, 256, 512	USI*	master, slave*	master, slave*	1 / 0 / 1	2 x 2	8	12	DIP-14N, SO150-14, QFN-20, VQFN-20, UFBGA-15	avr2.5	ISP, dW, HVSP	[13] [14] [15] [16] [17] [18]

ATtiny25, ATtiny25V, ATtiny45, ATtiny45V, ATtiny85, ATtiny85V	20, 10	2, 4, 8	128, 256, 512	128, 256, 512	USI*	master, slave*	master, slave*	2[19] / 0 / 0	2 x 2 [20][21]	4	6	DIP-8N, SO208-8, TSSOP-8, QFN-20	avr2.5	ISP, dW, HVSP	[22] [23] [24]
ATtiny43U	8	4	256	64	USI*	master, slave*	master, slave*	2 / 0 / 0	2 x 2	4	16	SO300-20, QFN-20	avr2.5	ISP, dW, HVPP	[25]
ATtiny48, ATtiny88	12	4, 8	256, 512	64	No	master, slave	master, slave	1 / 0 / 1	1 x 2	6 / 8	24, 28	DIP-28N, QFN-28, TQFP-32, QFN-32, UFBGA-32	avr2.5	ISP, dW, HVPP	[26] [27]
ATtiny87, ATtiny167	16	8, 16	512	512	USI*, UART*	No	master, slave	1 / 0 / 1	1 x 1	11	16	SO300-20, TSSOP-20, VQFN-32	avr2.5, avr35	ISP, dW, HVPP	[28] [29]
ATtiny261, ATtiny261A, ATtiny461, ATtiny461A, ATtiny861, ATtiny861A	20	2, 4, 8	128, 256, 512	128, 256, 512	USI*	master, slave*	master, slave*	1[30] / 0 / 1	1 x 3[31]	11	16	DIP-20N, SO300-20, TSSOP-20, QFN-32	avr2.5	ISP, dW, HVPP	[32] [33] [34] [35] [36]
ATtiny441, ATtiny841	16	4, 8	256, 512	256, 512	2 USART*	slave	master, slave	1 / 0 / 2	2 x 2	12	12	SO150-14, QFN-20, VQFN-20	avr2.5	ISP, dW, HVSP	[37] [38]
ATtiny828	20	8	512	256	USART*	slave	master, slave	1 / 0 / 1	2 x 2	28	28	TQFP-32, QFN-32	avr2.5	ISP, dW, HVPP	[39]
ATtiny1634	12	16	1024	256	USI*, 2 USART*	slave	master*	1 / 0 / 1	2 x 2	12	18	SO300-20, QFN-20	avr35	ISP, dW, HVPP	[40]
ATtiny2313, ATtiny2313V, ATtiny2313A, ATtiny4313	20	2, 4	128, 256	128, 256	USI*, USART*	master, slave*	master, slave*	1 / 0 / 1	2 x 2	No	18	DIP-20N, SO300-20, VQFN-20	avr2.5	ISP, dW, HVPP	[41] [42] [43] [44]
ATtiny4, ATtiny5, ATtiny9, ATtiny10	12	0.5 / 1	32	No	No	No	No	0 / 0 / 1	1 x 2	4 [45]	4	SOT23-6, UDFN-8	avrtiny10	TPI	[46] [47] [48] [49]
ATtiny20	12	2	128	No	No	slave	master, slave	1 / 0 / 1	2 x 2	8	12	SO150-14, TSSOP-14, VQFN-20, UFBGA-15, WLCSP-12	avrtiny10	TPI	[50]
ATtiny40	12	4	256	No	No	slave	master, slave	1 / 0 / 1	1 x 2	12	18	SO300-20, TSSOP-20, VQFN-20	avrtiny10	TPI	[51]
ATtiny102(F)	12	1	32	No	USART*	No	master*	0 / 0 / 1	yes	5	6	SO150-8, UDFN-8	?	TPI	[52]
ATtiny104(F)	12	1	32	No	USART*	No	master*	0 / 0 / 1	yes	9	12	SO150-14	?	TPI	[53]

ATtiny202, ATtiny402 (0-series)	20	2, 4	128, 256	64, 128	USART*	master, slave	master, slave	0 / 0 / 2 / R	yes	6	6	SO150-8	avrxmega3	UPDI	[54] [55]
ATtiny204, ATtiny404, ATtiny804, ATtiny1604 (0-series)	20	2, 4, 8, 16	128, 256, 512, 1024	64, 128, 256	USART*	master, slave	master, slave	0 / 0 / 2 / R	yes	10	12	SO150-14	avrxmega3	UPDI	[56] [57] [58] [59]
ATtiny406, ATtiny806, ATtiny1606 (0-series)	20	4, 8, 16	256, 512, 1024	128, 256	USART*	master, slave	master, slave	0 / 0 / 2 / R	yes	12	18	SO300-20, VQFN-20	avrxmega3	UPDI	[60] [61] [62]
ATtiny807, ATtiny1607 (0-series)	20	8, 16	512, 1024	128, 256	USART*	master, slave	master, slave	0 / 0 / 2 / R	yes	12	22	VQFN-24	avrxmega3	UPDI	[63] [64]
ATtiny212, ATtiny412 (1-series)	20	2, 4	128, 256	64, 128	USART*	master, slave	master, slave	0 / 1 / 2 / R	yes	6	6	SO150-8	avrxmega3	UPDI	[65] [66]
ATtiny214, ATtiny414, ATtiny814, ATtiny1614 (1-series)	20	2, 4, 8, 16	128, 256, 512, 2048	64, 128, 256	USART*	master, slave	master, slave	0 / 1 / 2 / R	yes	10	12	SO150-14	avrxmega3	UPDI	[67] [68] [69] [70]
ATtiny416, ATtiny816, ATtiny1616, ATtiny3216 (1-series)	20	4, 8, 16, 32	256, 512, 2048	128, 256	USART*	master, slave	master, slave	0 / 1 / 2or3 / R	yes	12	18	SO300-20, QFN-20, VQFN-20	avrxmega3	UPDI	[71] [72] [73] [74]
ATtiny417, ATtiny817, ATtiny1617, ATtiny3217 (1-series)	20	4, 8, 16, 32	256, 512, 2048	128, 256	USART*	master, slave	master, slave	0 / 1 / 2 / R	yes	12	22	VQFN-24, QFN-24	avrxmega3	UPDI	[75] [76] [77] [78]
ATtiny424, ATtiny824, ATtiny1624, ATtiny3224 (2-series)	20	4, 8, 16, 32	512, 1024, 2048, 3072	128, 128, 256, 256	2 USART*	yes	yes	0 / 0 / 3 / R	yes	9	12	SO-14, TSSOP-14	?	UPDI	[79] [80]
ATtiny426, ATtiny826, ATtiny1626, ATtiny3226 (2-series)	20	4, 8, 16, 32	512, 1024, 2048, 3072	128, 128, 256, 256	2 USART*	yes	yes	0 / 0 / 3 / R	yes	15	18	SO-20, SSTOP-20, VQFN-20	?	UPDI	[81] [82]
ATtiny427, ATtiny827, ATtiny1627, ATtiny3227 (2-series)	20	4, 8, 16, 32	512, 1024, 2048, 3072	128, 128, 256, 256	2 USART*	yes	yes	0 / 0 / 3 / R	yes	15	22	VQFN-24	?	UPDI	[83] [84]
Device (family)	Max clock (MHz)	Flash (KiB)	SRAM (bytes)	EEPROM (bytes)	UART	I²C (TWI (Two-wire interface))	SPI	Timers 8/12/16/R (bits)	PWM (Pulse-width modulated)	ADC pins	GPIO pins	IC Packages	GCC arch ID	Pgm Dbg	Refs

Notes

1. ↑ timers x waveform generators
2. ↑ timer0 can use clocks up to the core clock, timer1 can use clocks up to 64MHz
3. ↑ 4 pins are usable, but only 3 unique generators can be attached. The 4th pin would be the inverse of OC1B on the 3rd pin
4. ↑ Inverted outputs with configured dead zones can be set up for the 64MHz-capable timer1.
5. ↑ timer/counter1 is a 10-bit counter that can use clocks to 64MHz.

References

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2. 3rd pin x waveform generators
3. AVR compiler options; gcc.gnu.org https://gcc.gnu.org/onlinedocs/gcc/AVR-Options.html

- Timer PWM channels are based on the 10-bit counter with a maximum of 64MHz clock. Each PWM channel can generate two outputs, normal and inverted, on distinct IO pins. Each pair of outputs can be configured to have a dead-time between their on-states.
- ADC only on ATtiny5/10, and channels are 8 bits instead of 10
- Package column - the number after the dash is the number of pins on the package. **DIP** packages in this table are 0.3 inches (7.62 mm) row-to-row. **SO**www means SOIC package with a case width of 'www' in thousandth of an inch. Through-hole package types are mostly by more than one name, a convenience was only added to make it easier to compare packages.
- UART/I²C/SPI columns - green cell means a dedicated peripheral, * yellow cell means a multi-feature peripheral that is chosen by setting configuration bits. Most USART peripherals support a minimum choice between UART or SPI, where as some might support additional choices, such as LIN, IrDA, RS-485.
- Timers column - recent families add a 12-bit timer, plus a 16-bit Real Time Counter (RTC) that is driven by a 32.768kHz clock (feature designated with 'R' in the table).
- ADC chans column - the total number of analog channels that are multiplex into the ADC input. Most parts have one ADC, a few have two ADC.
- Pgm/Dbg column - flash programming and debugging protocols: **HVPP** means High Voltage Parallel Programming 12V protocol. **HVSP** means High Voltage Serial Programming 12V protocol. **ISP** means In-System Programmable protocol, uses SPI to program the internal flash. **TPI** is Tiny Programming Interface. **dW** means debugWIRE protocol. **UPDI** means Unified Program and Debug Interface protocol (newest).[85]

Abbreviations:

- Many of Atmels microcontrollers contain built-in support for interfacing to a two-wire bus, called Two-Wire Interface. This is essentially the same thing as the I²C interface by Philips, but that term is avoided in Atmel's documentation due to trademark issues.
- USI: Universal Serial Interface (not to be confused with USB). The USI is a multi-purpose hardware communication module. With appropriate software support, it can be used to implement an SPI,[86] I²C[87][88] or UART[89] interface. USART peripherals have more features than USI peripherals.

2. Timeline

The following table lists each ATtiny microcontroller by the first release date of each datasheet.

Year	Device (family)
1999	**ATtiny11, ATtiny11L, ATtiny12, ATtiny12L, ATtiny12V, ATtiny22, ATtiny22L**
2002	**ATtiny15L, ATtiny26, ATtiny26L, ATtiny28L, ATtiny28V**
2003	**ATtiny13, ATtiny13V, ATtiny2313, ATtiny2313V, ATtiny4313**
2005	**ATtiny24, ATtiny24V, ATtiny25, ATtiny25V, ATtiny44, ATtiny44V, ATtiny45, ATtiny45V, ATtiny84, ATtiny84V, ATtiny85, ATtiny85V**
2006	**ATtiny261, ATtiny461, ATtiny861**
2008	**ATtiny13A, ATtiny24A, ATtiny44A, ATtiny48, ATtiny84A, ATtiny88**
2009	**ATtiny4, ATtiny5, ATtiny9, ATtiny10, ATtiny43U, ATtiny261A, ATtiny461A, ATtiny861A, ATtiny2313A**
2011	**ATtiny20, ATtiny40, ATtiny87, ATtiny167**
2011	**ATtiny1634**
2012	**ATtiny441, ATtiny841, ATtiny828**
2016	**ATtiny102(F), ATtiny104(F), ATtiny417, ATtiny817**
2017	**ATtiny212, ATtiny412, ATtiny214, ATtiny414, ATtiny814, ATtiny416, ATtiny816**
2018	**ATtiny202, ATtiny402, ATtiny204, ATtiny404, ATtiny804, ATtiny1604, ATtiny406, ATtiny806, ATtiny1606, ATtiny807, ATtiny1607, ATtiny1614, ATtiny1616, ATtiny3216, ATtiny1617, ATtiny3217**
2020	**ATtiny1624, ATtiny1626, ATtiny1627**
2021	**ATtiny424, ATtiny824, ATtiny426, ATtiny826, ATtiny427, ATtiny827**

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16. timer0 can use clocks up to the core clock, timer1 can use clocks up to 64MHz
17. 4 pins are usable, but only 3 unique generators can be attached. The 4th pin would be the inverse of OC1B on the 3rd pin.
18. Inverted outputs with configured dead zones can be set up for the 64MHz-capable timer1
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27. timer/counter1 is a 10-bit counter that can use clocks to 64MHz.

3. Development Boards

The following are ATtiny development boards sold by Microchip Technology:

- ATtiny104 Xplained Nano
- ATtiny416 Xplained Nano
- ATtiny817 AVR Parrot
- ATtiny817 Xplained Mini
- ATtiny817 Xplained Pro
- ATtiny3217 Xplained Pro

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