Cubic Silicon Carbide

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The cubic silicon carbide is the only polytype that can be grown on silicon wafers. This approach reduces the cost as no SiC substrate is used and only the silicon carbide layer thickness required for the specific application is grown on a cheaper Si substrate. This technology also offers the potential for faster scale-up with wafer size compared with the development of larger diameter hexagonal SiC wafers. In principle, with a large reactor, a 300 mm Si wafer can be obtained using the present process.

Keywords: 3C-SiC ; heteroepitaxy ; bulk growth ; compliant substrates ; defects ; stress

1. Introduction

Wide band-gap (WBG) semiconductor devices based on both silicon carbide (SiC) and gallium nitride (GaN) can lead a revolution in power electronics through its faster switching speeds, lower losses, and higher blocking voltages [1]. Furthermore, their properties enable higher operating temperatures and increased power densities, but until now the benefits shown by WBG power electronics have not been fully realized due to the high costs of the material and reliability challenges.

Silicon carbide is a material presenting different crystalline structures called polytypes [2]. To date, only the two hexagonal structures 4H and 6H-SiC are commercialized, while the cubic form (3C-SiC) is not used until now in power devices despite the large effort of the last years and several hundreds of papers published for each year. All these polytypes have similar benefits over silicon such as higher breakdown fields (2–4 MV/cm) and the larger energy band-gap (2.3–3.2 eV).

Both 3C-SiC and GaN can work in the same breakdown voltage range (200–1200 V). 3C-SiC is more appropriate for high-current applications due to its high thermal conductivity, while GaN better fits in RF applications because of the high saturated electron velocity. The lower band-gap of 3C-SiC (2.3 eV) in comparison to 4H-SiC (3.28 eV) is often viewed as a negative aspect with respect to other polytypes. The lower band-gap brings a positive effect because the lowering of the conduction band minimum causes a reduced density of states at the SiO 2/3C-SiC interface [3]. As a consequence, it has been demonstrated that the metal oxide semiconductor field effect transistor (MOSFET) on 3C-SiC has the highest channel mobility (above 300 cm 2/V/s) ever presented on any SiC polytype [4]. This produces a large reduction in the power consumption of power switching devices [5]. A remaining challenge in both 3C and 4H-SiC is the electrical activity of extended defects. It is identified as the major problem for electronic device functionality. The mechanisms of defect formation must be clarified and the methods for their reduction developed to reach full functionality and high yield [6]. So far, the growth of 3C-SiC on silicon has been demonstrated on 150 mm Si wafers [7][8]. The process is feasible with up-scaled reactors on 200 mm or 300 mm wafers.

Another problem to solve concerns the intrinsic stress created during the growth process due to the lattice mismatch between 3C-SiC (4.36 Å) and Si (5.43 Å) [9]. Thermo-elastic stress also appears at the post-deposition cooling due to the 8% difference in the thermal expansion coefficients between these two materials [10]. This results in stress which induces the formation of various planar or extended defects in 3C-SiC. These defects produce a considerable degradation of the crystalline quality of the epitaxial layer [11].

There are two types of defects in the epitaxial 3C-SiC layers. Anti-phase boundaries (APBs) are planar defects that are formed at the geometrical separation of two 3C-SiC grains. The grain differs by a 90° rotation in the Si(100) growth plane [12]. These are described as anti-phased domains (APDs) that are formed by the steps present on the Si surface. A second defect type is the stacking fault along the {111} planes. Most research work highlights the intrinsic nature of these defects and points out that a reduction of their density is possible by increasing the film thickness. The electrical activity of the extended defects in 3C-SiC is a dominant problem for electronic device performance. Clearly, a reduction of these defects is essential to improve the yield of power electronic devices [13].

In the last years during the CHALLENGE project [14], we have been active in developing two different approaches. In the first one, we have used several structured substrates (compliance substrates) [15][16][17] to reduce the defect density and stress. This approach maintains the attractive low cost of the silicon substrate material. However, it does not take advantage of the high heat dissipation of 3C-SiC because it is limited by the low thermal conductivity of silicon. The second approach of the bulk growth has a higher cost due to the higher cost of the 3C-SiC substrate but allows to take advantage of the high thermal conductivity of 3C-SiC in the devices. Furthermore, there is an advantage in the device processing because of the possibility to use the high-temperature processes already developed in 4H-SiC processing (e.g., epitaxy, ion implantation activation, etc.). The use of Si as a substrate has the main advantage, with respect to 4H-SiC, of reaching large diameters directly without the long and expensive process of the traditional diameter enlargement. In addition, the lower band-gap and higher channel mobility of 3C-SiC can produce MOSFET with a lower R_{on} with respect to both Si and 4H-SiC in the breakdown voltage region between 200 and 1200 V [5]. In previous works [18][19], it was observed that in increasing the grown thickness of the material, the density of SFs can be strongly reduced and this will produce an overall improvement in the electrical performance of the devices.

The bulk growth of hexagonal 6H and 4H silicon carbide polytypes can be considered mature while the same cannot be said about the cubic polytype (3C-SiC) [20][21]. Different approaches such as the modified PVT (Physical Vapour Transport) (M-PVT) or continuous-feed PVT (CF-PVT) method have been presented for bulk growth over the last decade [22][23][24]. Only the methods based on the sublimation sandwich implemented by Tairov et al. [25] could allow for the formation of 3C-SiC [6][26]. A major drawback for all the mentioned bulk growth processes is the lack of available high-quality seeding material. One widely investigated approach makes use of hexagonal SiC wafer materials and explores switching to 3C-SiC. Another promising approach is based on the heteroepitaxial growth of cubic silicon carbide on silicon (3C on Si) using chemical vapor deposition (CVD). This method faces some challenges caused by the lattice mismatch of approximately 20% between silicon and 3C-SiC, and the difference in thermal expansion [27]. The research in this area has advanced in major ways over the last years and has been revitalized to use the material as seed for bulk growth processes [6].

2. New Approaches and Understandings in the Growth of Cubic Silicon Carbide

In the CHALLENGE project, two main different approaches were used to grow 3C-SiC. From one hand, several compliance substrates (pillars, SiGe buffer layer, ISP, etc.) were used to reduce both defects and stress. On the other hand, new bulk growth techniques (PVT or CVD) have been developed to improve the quality of this material. During this work, a new understanding of the defects in this material (protrusions, APBs, SFs, and point defects), their interactions, and the effect of the growth process on their formation and reduction have been obtained. This new understanding has been also helped by the simulation codes developed inside the project (KMCsL, MD, phase field, etc.) and by new characterization techniques (C-AFM).

From this large study on the growth of 3C-SiC, several conclusions can be reported: The use of the SiGe buffer layer is interesting and in some cases, some good quality samples can be obtained. The main limitation is that a low-temperature growth should be used and the Ge segregation at the 3C-SiC/Si interface can produce the formation of polycrystalline regions. The process window is narrow and thus this process can be difficult to use in a production line. The ISP substrate produces a fast decrease of the SFs' density, as reported in the previous papers, but at the same time produces the formation of APBs that can be detrimental for the leakage current of the devices, as observed by C-AFM measurements. To decrease the APBs concentration, a very high thickness can be grown or new ISP structures should be realized. The pillar substrates have demonstrated to be extremely interesting in reducing the stress and bow of the wafer, especially for (111) substrates. On this kind of substrate, even 25–30 μm of the 3C-SiC layer could be grown without cracks and with a low bow. The main problem of this process is that the 3D growth of 3C-SiC is not easy to control and thick layers are needed to obtain a continuous substrate. This kind of technology can be interesting in the future when a good 3C-SiC (111) layer should be realized. During the last years, we developed a carbonization process that decreases the voids almost to zero at the 3C-SiC/Si interface with a considerable improvement of the material quality and a decrease of the stress. Even the growth during the temperature ramp (buffer layer) between the carbonization and growth steps has a large effect on the stress. The main part of the investigation of the last years has been on the study of the evolution of SFs and APBs, as well as their interactions. The different types of SFs (SF<1>, SF<2>, SF<3>), their generation and annihilation, and the influence of the PD on these processes have been observed and studied in great detail. Another aspect that has been studied in detail is the interaction between the APBs and SFs. In fact, APBs can both generate or annihilate SFs and all these processes have been studied both experimentally and by simulations. It has been observed that due to this equilibrium between the generation and recombination of SFs, very thick layers are needed to obtain a low value of SFs that can provide the opportunity to realize a good device on 3C-SiC. The growth conditions (growth

temperature, growth rate, and doping) can influence this equilibrium between generation and annihilation. It seems also that the different types of SFs have different behaviors during the growth but more investigations on this aspect are needed. From these studies, it has been understood that the bulk growth of 3C-SiC is needed to obtain a low value of defects compatible with the realization of power devices. We have developed different kinds of growth techniques (CVD and PVT) to realize bulk wafers with dimensions compatible with the actual standards (100 and 150 mm) but the main problem is related to the formation of the protrusions in the first instant of the growth. This 3D defect can grow and cover the entire surface of the ingot, thus a new process that can eliminate the formation of these defects is needed to obtain a 3C-SiC wafer for the realization of power devices. Another aspect of the 3C-SiC bulk growth that needs further investigation is the intrinsic stress of this material. In fact, the high level of stress and bow of the wafers are a problem for the further processing of the 3C-SiC wafers.

Further work should be done to obtain a good material for power devices, but the work performed during this project is a fundamental step for developing new materials for power devices.

References

1. Chow, T.P. High-voltage SiC and GaN power devices. Microelectron. Eng. 2006, 83, 112–122.
2. Pensl, G.; Ciobanu, F.; Frank, T.; Krieger, M.; Reshanov, S.; Schmid, F.; Weidner, M. SiC material properties. Int. J. Hig h Speed Electron. Syst. 2005, 15, 705–745.
3. Schöner, A.; Krieger, M.; Pensl, G.; Abe, M.; Nagasawa, H. Fabrication and Characterization of 3C-SiC-Based MOSFE Ts. Chem. Vap. Depos. 2006, 12, 523–530.
4. Uchida, H.; Minami, A.; Sakata, T.; Nagasawa, H.; Kobayashi, M. High Temperature Performance of 3C-SiC MOSFETs with High Channel Mobility. Mater. Sci. Forum 2012, 717, 1109–1112.
5. Van Zeghbroeck, B.; Fardi, H. Comparison of 3C-SiC and 4H-SiC Power MOSFETs. Mater. Sci. Forum 2018, 924, 774 –777.
6. La Via, F.; Severino, A.; Anzalone, R.; Bongiorno, C.; Litrico, G.; Mauceri, M.; Schoeler, M.; Schuh, P.; Wellmann, P. Fro m thin film to bulk 3C-SiC growth: Understanding the mechanism of defects reduction. Mater. Sci. Semicond. Process. 2018, 78, 57–68.
7. Severino, A.; Locke, C.; Anzalone, R.; Camarda, M.; Piluso, N.; la Magna, A.; Saddow, S.E.; Abbondanza, G.; D'Arrigo, G.; La Via, F. 3C-SiC film growth on Si substrates. ECS Transact. 2011, 35, 99–116.
8. Wang, L.; Dimitrijev, S.; Han, J.; Iacopi, A.; Hold, L.; Tanner, P.; Harrison, H.B. Growth of 3C–SiC on 150-mm Si(100) su bstrates by alternating supply epitaxy at 1000 °C. Thin Solid Film. 2011, 519, 6443–6446.
9. Anzalone, R.; D'Arrigo, G.; Camarda, M.; Locke, C.; Saddow, S.E.; La Via, F. Advanced Residual Stress Analysis and F EM Simulation on Heteroepitaxial 3C–SiC for MEMS Application. J. Microelectromech. Syst. 2011, 20, 745–752.
10. Iacopi, F.; Walker, G.; Wang, L.; Malesys, L.; Ma, S.; Cunning, B.V.; Iacopi, A. Orientation-dependent stress relaxation i n hetero-epitaxial 3C-SiC films. Appl. Phys. Lett. 2013, 102, 011908.
11. Zielinski, M.; Ndiaye, S.; Chassagne, T.; Juillaguet, S.; Lewandowska, R.; Portail, M.; Leycuras, A.; Camassel, J. Strain and wafer curvature of 3C-SiC films on silicon: Influence of the growth conditions. Phys. Stat. Sol. 2007, 204, 981–986.
12. Nagasawa, H.; Yagi, K.; Kawahara, T.; Hatta, N. Reducing Planar Defects in 3C–SiC. Chem. Vap. Depos. 2006, 12, 50 2–508.
13. Nagasawa, H.; Abe, M.; Yagi, K.; Kawahara, T.; Hatta, N. Fabrication of high perfor-mance3C-SiC vertical MOSFETs by reducing planar defects. Phys. Stat. Sol. 2008, 245, 1272–1280.
14. La Via, F.; Roccaforte, F.; La Magna, A.; Nipoti, R.; Mancarella, F.; Wellmann, P.J.; Crippa, D.; Mauceri, M.; Ward, P.; Mi glio, L.; et al. 3C-SiC Hetero-Epitaxially Grown on Silicon Compliance Substrates and New 3C-SiC Substrates for Sust ainable Wide-Band-Gap Power Devices (CHALLENGE). Mater. Sci. Forum 2018, 924, 913–918.
15. Albani, M.; Marzegalli, A.; Bergamaschini, R.; Mauceri, M.; Crippa, D.; La Via, F.; von Känel, H.; Miglio, L. Solving the cr itical thermal bowing in 3C-SiC/Si(111) by a tilting Si pillar architecture. J. Appl. Phys. 2018, 123, 185703.
16. Zimbone, M.; Zielinski, M.; Barbagiovanni, E.G.; Calabretta, C.; La Via, F. 3C-SiC grown on Si by using a Si1-xGex buff er layer. J. Cryst. Growth 2019, 519, 1–6.
17. Zimbone, M.; Zielinski, M.; Bongiorno, C.; Calabretta, C.; Anzalone, R.; Scalese, S.; Fisicaro, G.; La Magna, A.; Mancar ella, F.; La Via, F. 3C-SiC Growth on Inverted Silicon Pyramids Patterned Substrate. Materials 2019, 12, 3407.

18. Severino, A.R.; Anzalone, M.; Camarda, N.; Piluso, F.; La Via, F. Structural characterization of heteroepitaxial 3C-SiC. Mater. Sci. Forum 2012, 711, 27–30.
19. Polychroniadis, E.; Syväjärvi, M.; Yakimova, R.; Stoemenos, J. Microstructural characterization of very thick freestandin g 3C-SiC wafers. J. Cryst. Growth 2004, 263, 68–75.
20. Wellmann, P.; Neubauer, G.; Fahlbusch, L.; Salamon, M.; Uhlmann, N. Growth of SiC bulk crystals for application in po wer electronic devices—Process design, 2D and 3D X-ray in situ visualization and advanced doping. Cryst. Res. Techn ol. 2015, 50, 2–9.
21. Wellmann, P.J. Review of SiC crystal growth technology. Semicond. Sci. Technol. 2018, 33, 103001.
22. Chaussende, D.; Mercier, F.; Boulle, A.; Conchon, F.; Soueidan, M.; Ferro, G.; Mantzari, A.; Andreadou, A.; Polychronia dis, E.; Balloud, C.; et al. Prospects for 3C-SiC bulk crystal growth. J. Cryst. Growth 2008, 310, 976–981.
23. Jokubavicius, V.; Yazdi, G.R.; Liljedahl, R.; Ivanov, I.G.; Sun, J.; Liu, X.; Schuh, P.; Wilhelm, M.; Wellmann, P.; Yakimov a, R.; et al. Single Domain 3C-SiC Growth on Off-Oriented 4H-SiC Substrates. Cryst. Growth Des. 2015, 15, 2940–294 7.
24. Jokubavicius, V.; Yazdi, G.R.; Liljedahl, R.; Ivanov, I.G.; Yakimova, R.; Syväjärvi, M. Lateral enlargement growth mecha nism of 3C-SiC on off-oriented 4H-SiC substrates. Cryst. Growth Des. 2014, 14, 6514–6520.
25. Tairov, Y.; Tsvetkov, V.; Lilov, S.; Safaraliev, G. Studies of growth kinetics and polytypism of silicon carbide epitaxial laye rs grown from the vapour phase. J. Cryst. Growth 1976, 36, 147–151.
26. Schuh, P.; La Via, F.; Mauceri, M.; Zielinski, M.; Wellmann, P. Growth of Large-Area, Stress-Free, and Bulk-Like 3C-SiC (100) Using 3C-SiC-on-Si in Vapor Phase Growth. Materials 2019, 12, 2179.
27. Anzalone, R.; Litrico, G.; Piluso, N.; Reitano, R.; Alberti, A.; Fiorenza, P.; Coffa, S.; La Via, F. Carbonization and transiti on layer effects on 3C-SiC film residual stress. J. Cryst. Growth 2017, 473, 11–19.
