Layer-Scale Transfer Techniques

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Contributor: Zheng Gong

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layer transfer chip transfer hetero-integration

1. Layer Transfer Techniques

Layer transfer is a technique to transfer a layer of a particular semiconductor material, often of a wafer-scale size, from the original substrate to the target substrate of interest. The key process is to remove the growth substrate on which the semiconductor layer is deposited. The technique allows the integration of both lattice-matched and mismatched material systems for enabling extended functionality and performance by assembling diverse materials or devices in a more compact space. The additional benefit is the potential reuse of the growth substrate if it is not damaged during lift-off, thereby reducing the cost [1][2][3]. As one example, the transfer of GaN micro-LEDs onto silicon complementary metal oxide semiconductor (CMOS) allows a high-quality display with additional functionality such as pulse control.

The conventional method for layer transfer is mainly based on wafer bonding and mechanical thinning [4][5][6][7]. However, thinning techniques are difficult for accurate control of the film thickness and surface roughness across the wafer. For instance, in most cases, reducing the layer thickness down to 10 μm by mechanical thinning is extremely challenging. To address these challenges, a variety of new lift-off technologies have been developed to assist the wafer-scale layer transfer, some of which have the potential for volume production. These include epitaxial lift-off (ELO), mechanical spalling, laser lift-off, and ion cutting, as schematically shown in Figure 1 below.

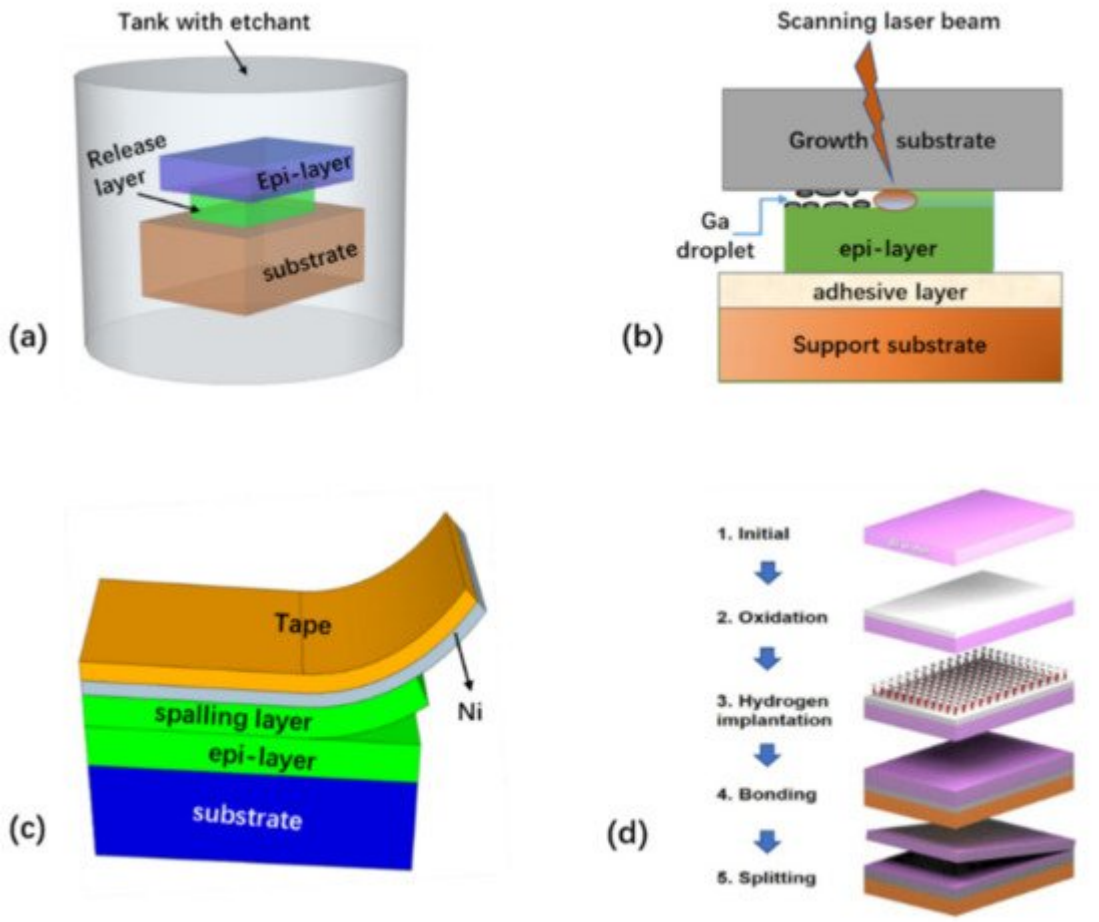

Figure 1. Sketches of common layer transfer techniques: (**a**) chemical epitaxial lift-off, (**b**) laser lift-off, (**c**) mechanical spalling, and (**d**) ion cutting.

2. Layer Transfer by Epitaxial Lift-off (ELO)

Referring to Figure 1a, ELO relies on the removal of a releasable or sacrificial layer introduced in the epi-stacks using various chemical etchants, such that the epi-layer on top of the releasing layer can be transferred to other substrates while preserving the original growth substrate [8][9][10][11][12][13][14][15][16][3][17][18][19][20][21][22][23][24][25][26][27][28][29][30][31][32][33][34][35][36][37][38][39][40][41][42][43][44][45][46][47][48][49][50][51][52][53][54][55][56][57][58][59][60][61][62][63][64][65]. The primary requirements for this technique are: (i) high etch selectivity of the releasing layer, (ii) the capability for high-quality growth of the epi-layer on the releasing layer, and (iii) minimized damage to the epi-layer after release. Therefore, the suitable release layer not only determines the epi-layer quality, but also determines the ELO quality. Selecting the right release layer is highly dependent on the epi-layer (to be released), substrate, and etchant solvent to be used. Commonly, chemical lift-off of small samples is relatively quick, but wafer-level release remains challenging. Depending on the specific release layer in the epi-stack, the etching duration for releasing the full wafer may vary from a few hours to a few days, which may impose practical limitations for large-volume production. Therefore, to accelerate the release, several variants of the conventional ELO have been proposed, including weight-assisted, surface tension force-assisted, or roller-assisted ELO techniques [3][51][52].

2.1. ELO Assisted by Lattice-Matched Release Layer

Earlier ELO studies of III-V semiconductor layers in the past were mainly based on lattice-matched release layers, primarily because the growth of high-quality layered semiconductors on a lattice-matched release layer is much easier than on a dissimilar sacrificial layer. Depending on the specific epitaxial structures and the growth substrate, the release layer and corresponding etching solvent can be quite different. For example, one common release layer for III-V semiconductors grown on GaAs is AlAs [55], which is a material lattice- matched with the substrate and can be removed by hydrofluoric acid. However, a recent investigation reveals that etching AlAs using hydrofluoric acid is fast, but it leads to reaction residuals and increased roughness of the released layer and substrate [3]. To alleviate this issue, lattice-matched AlInP was introduced to act as the release layer, which can be etched by a different solvent, hydrochloride acid [3]. In the latter case, very smooth III-V layers and substrate free from residuals can be achieved via a modified ELO technique termed as “surface tension-assisted ELO”, enabling the prospect of substrate reuse (Figure 2). In the case of InP-based nanomembranes grown on InP substrates, InGaAs was found to be a desirable sacrificial layer, which can be selectively etched by either HF+H_2O_2 [58] or H_3PO_4 and H_2O_2 [66]. Alternatively, InAlAs was also explored for releasing InP-based devices, which has higher etch selectivity, and less dependence on the crystal orientation caused by the etching solvent, compared with InGaAs [46]. In all cases, the release layer and corresponding etching solvent are chosen such that the semiconductor layer to be released maintains high epitaxy quality while the etch selectivity is high.

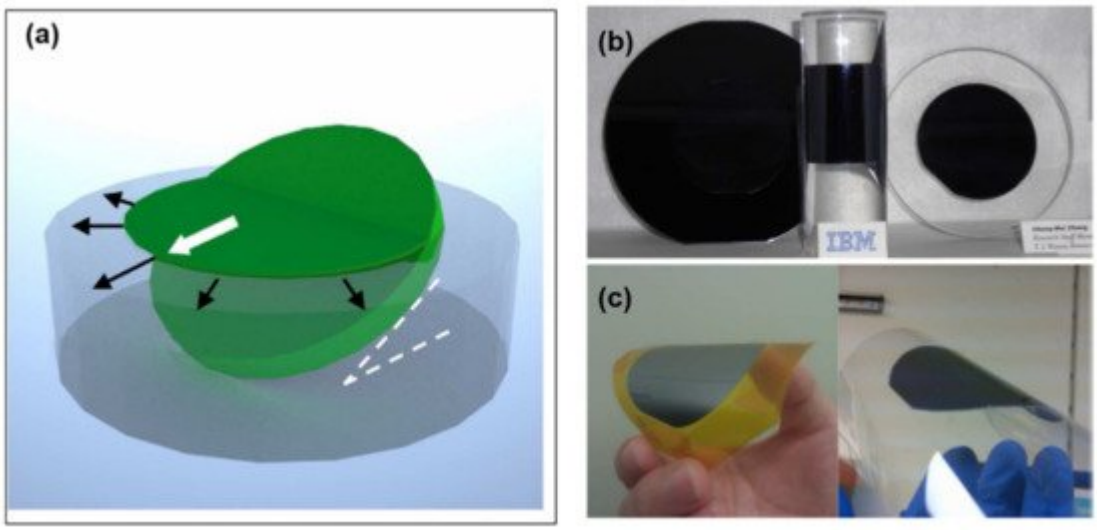

Figure 2. (**a**) Sketch of surface tension-assisted epitaxial lift-off (ELO) transfer techniques. (**b**) Demonstrations of the transferred GaAs thin films to the rigid substrate (left image, GaAs on 4” Si wafer. Center image, GaAs on curved solid object. Right image, GaAs on glass) and (**c**) flexible substrates (left, GaAs on tape. Right, GaAs on flexible sheet). Adapted from [3].

Releasing III-V semiconductor layers from the growth substrate to a receiving substrate by ELO has been researched for many years, and can be dated back to 1978. The ELO technique based on a lattice-matched release layer is now well developed, particularly for high-efficiency III-V solar cells [67][19][68][69].

2.2. ELO Assisted by Heterogeneous Release Layer

More recently, dissimilar release layers have also been explored, particularlyfor III-nitride layer release. Similar to III-V semiconductors, releasing III-nitride by ELO is also possible, but more challenging. Unlike III-V semiconductors, III-nitride layers themselves are resistant to most of etchant solvents and, therefore, they are not ideal release layers for GaN. To overcome this limit, most of efforts are therefore focused on introducing a dissimilar release layer rather than GaN alloy into the III-nitride epi-stack for ELO [17][20][30][32][41][42][44][45][50][60]. However, the epitaxial growth of GaN on a heterogeneous release layer is more challenging, and may lead to degraded material quality due to the lattice mismatch. Despite of these challenges, various release layers, including SiO_2 [17][20][60], Ga_2O_3 [32], CrN [30], Nb_2N [45], AlN [41][42], and ZnO [44][50], have been successfully explored to lift off GaN membranes.

Hsueh et al. demonstrated the use of ZnO as a sacrificial layer [50]. A 2-inch ZnO template layer was grown on a sapphire substrate by using pulsed laser deposition (PLD). The wafer was then loaded into an hydride organometallic vapor phase epitaxy (HOVPE) chamber for further growth of GaN epi-layers on top of the ZnO release layer. A low-pressure/temperature HOVPE approach was adopted to prevent ZnO decomposition. The completed wafer was then fixed onto a glass support using wax. Afterward, ELO was performed using HCL as an etchant solvent, resulting in the entire transfer of the 2-inch GaN epi-layer to the support substrate without apparent degradation of the GaN epi-layer. Due to the lateral etching mechanism, the etch rate at the wafer edge was found to be faster than in the wafer center. The surface of the released substrate was found to be very smooth, opening up the prospect of substrate reuse and cost reduction.

As another example of suitable release layers for GaN lift-off, CrN [30] was formed on a sapphire substrate by depositing chromium with a radio frequency (RF) sputtering system, followed by a nitridation process. LED layer structures were then grown on the CrN buffer/substrate by low-pressure HOVPE. A gold layer was electroplated to the p-GaN side to act as the support substrate. By selectively etching the CrN release layer using a mixture of H_2O, $Ce(NH4)_2$ $(NO_3)_6$, and $HClO_4$, high-performance vertical LEDs transferred onto a gold support can be achieved. It was found that such vertical LEDs have much smaller serial resistance, showing the potential for general lighting. However, in this particular work, only centimeter-scale lift-off was realized. Whether it is suited for wafer-level ELO remains an open question.

Hsueh et al. demonstrated the use of Ga_2O_3 [32] as a release layer for III-nitride lift-off. LED layers grown on Ga_2O_3 can then be readily removed by HF, resulting in the transfer of 2-inch GaN LEDs to the electroplated Cu support. As GaN is inert to HF etching, the LED layer experiences minimal damage. One disadvantage of Ga_2O_3 is its decomposition under high temperatures in a H_2-rich environment. Therefore, Ga_2O_3 must be grown separately in a N-rich atmosphere.

While various dissimilar release layer-assisted ELO techniques have been explored, great challenges remain for releasing III-nitride semiconductors. Thus far, the feasibility for commercial production of nitride compound semiconductors based on release layer-assisted ELO is not proven yet. The major challenges are relevant to the

compromised epitaxy quality grown on a dissimilar sacrificial layer, and the etching-induced damage to the semiconductor layer to be released.

2.3. ELO Assisted by Micro/Nanopatterned Structures

In some cases, micro/nanopatterned structures can be used to assist the layer transfer [17]. In one example, nanoporous SiO_2 [60] is formed by using an anodized alumina template as a mask. A GaN epi-layer is then grown on top of the nanoporous SiO_2. After finishing the growth, wet etching of the nanoporous SiO_2 using HF is performed, leading to the spontaneous release of the GaN film. The nanoporous SiO_2 also facilitates the lateral epitaxial growth of high-quality GaN on the nanoporous SiO_2, which can reduce the dislocation density in the epi-layer.

Void microstructures are also utilized to assist the layer release [18][42]. Lin et al. [42] demonstrated the growth of nitride semiconductors on a truncated triangle striped pattern sapphire substrate (Figure 3). This leads to the formation of an epi-stack with embedded void structures. These voids facilitate the wet etching of a thin AlN sacrificial layer in the lateral direction by hot KOH etching, leading to the formation of released GaN layers.

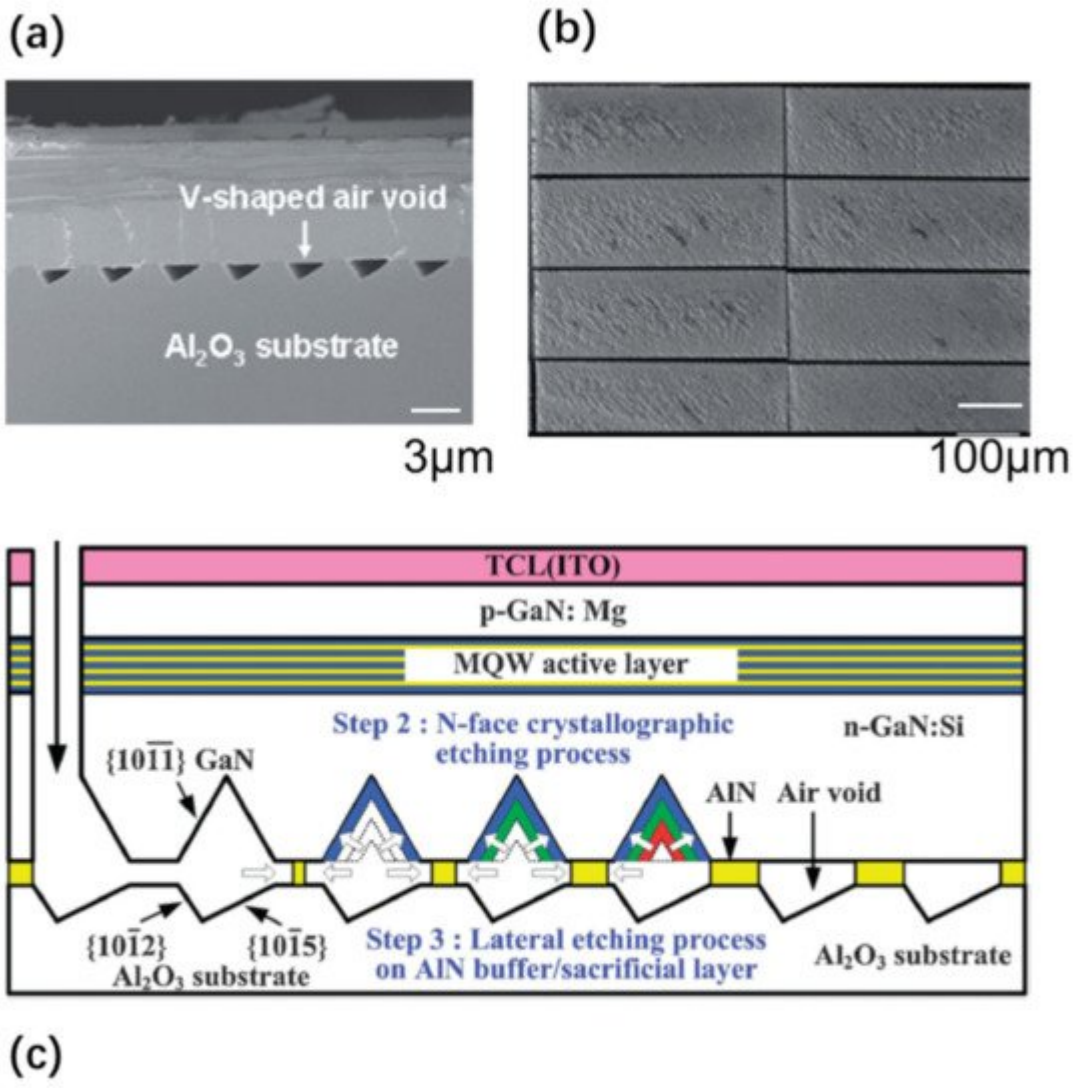

Figure 3. (**a**) An LED epitaxial layer was grown on the patterned sapphire substrate with V-shaped void channels. (**b**) The individual LED chips defined through the laser scribing process were lifted off from the void structures. (**c**) Schematic diagram of the multiple-quantum-well (MQW) LED structure topped with a transparent conductive layer (TCL) ITO for the chemical lift-off (CLO) process. Adapted with permission of [42]. Copyright Applied Physics Express, 2010.

2.4. Photoelectrochemical (PEC) or Electrochemical (EC) Etching

PEC etching methods [8][9][11][24][31][35][43][47][48][57][59][63] have been developed to release III-nitride, although conventional wet etching is difficult for etching III-nitride. This method exploits the illumination that only absorbs in the specific layer, in order to form electron–hole pairs in the semiconductor material [59]. The photogenerated holes result in the oxidation and dissolution of the semiconductor layer, while the electrons are moved to the cathode to participate in a reduction reaction. An example of PEC etching is demonstrated by Youtsey et al. [59]. The detailed PEC etching procedure is shown in Figure 4a. By selective PEC etching of an InGaN release layer, wafer-scale lift-off of 4-inch GaN films was demonstrated (Figure 4b).

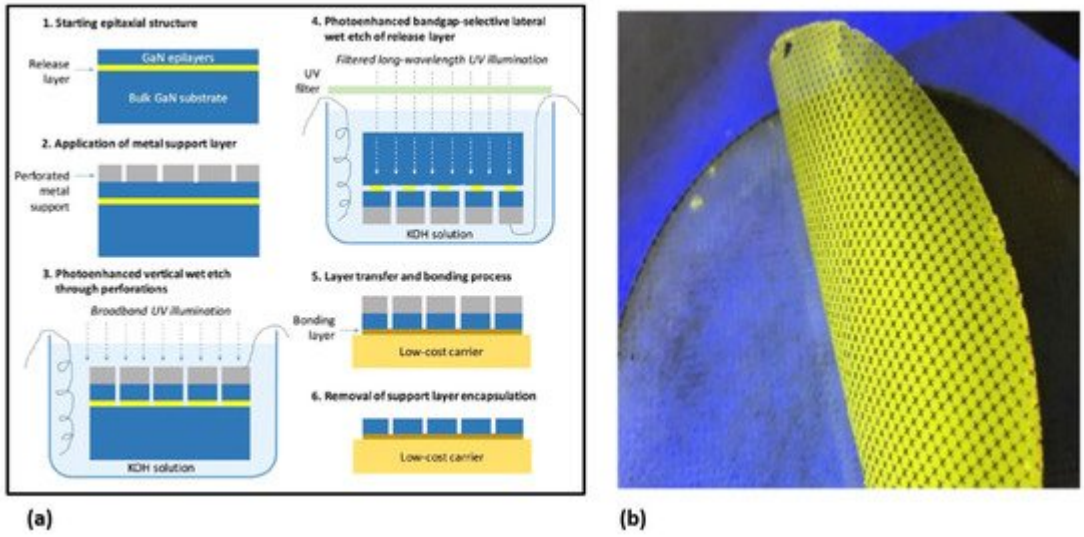

Figure 4. (**a**) The detailed process flow of ELO based on photoelectrochemical (PEC) etching, and (**b**) full 4-inch GaN layer released by PEC etching. Adapted with permission from [59]. Copyright John Wiley and Sons, 2017.

In 2011, Lin et al. reported the lift-off of InGaN LED structures using a hybrid approach of PEC etching and mechanical peeling [43]. LED structures are prepatterned and fabricated on a sapphire substrate, followed by PEC lateral etching of the InGaN/GaN superlattices. A tape is then laminated onto the LED top. Mechanical peeling of the tape allows LEDs to be successfully transferred to the tape, with the emission blueshift to a shorter wavelength due to the strain relaxation. In a more recent work [11], similar PEC etching is conducted to release nanopillar LEDs defined by nanosphere lithography.

One of the disadvantages of PEC etching methods, however, is the requirement of external illumination sources. To address this issue, EC etching techniques without light illumination have also bene developed. For instance, Park

et al. developed a method based on dope-selective EC etching to release GaN membranes [47]. The EC etching is fast for n-GaN but it is almost inert for p-GaN and undoped GaN. Making use of this highly selective etching, successful lift-off of patterned p-GaN films was achieved.

Modified EC etching methods for GaN release have also been developed [64]. Porous GaN formed by EC etching is exploited to assist the lift-off, whose porosity can be tuned by changing the doping concentration and adjusting the etching voltage. Zhang et al. [64] developed two different schemes for GaN layer transfer (Figure 5). In the first procedure (i.e, Procedure A shown in Figure 5a), two-stage EC etching was applied to n-doped GaN. Initially, a lower bias is applied to the GaN, and results in the formation of a porous GaN film of a certain depth. The bias is then increased in the second stage, leading to the formation of a void layer with larger porosity exactly below the porous layer generated in the first stage. Consequently, the GaN film can be released from the substrate. Alternatively, GaN release is also demonstrated based on a GaN sample with lightly doped n-GaN and heavily doped n-GaN, but only a constant bias is applied for conducting EC etching (Procedure B in Figure 5b). In this case, a void layer with larger porosity can be formed below lightly doped GaN. In both cases, centimeter-scale free-standing GaN membranes without degradation have been achieved. In the latter case, the thickness of the transferred layer can be accurately controlled by the doping concentration. However, wafer-scale release of GaN based on EC etching remains challenging.

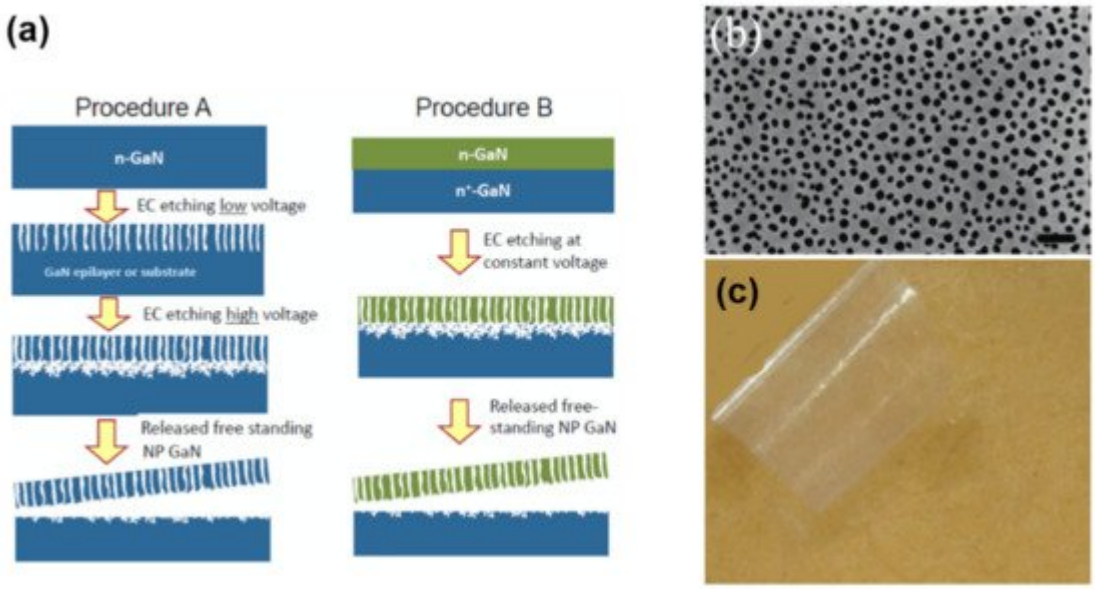

Figure 5. (**a**) Sketches of two different EC etching procedures, (**b**) SEM image of the porous structures formed by EC etching, and (**c**) the GaN membrane released from the porous GaN layer formed by EC etching. NP GaN in (a) stands for the nanoporous GaN. Adapted with permission from [64]. Copyright IOP Publishing, 2010.

In the above, successful lift-off of a single doped GaN layer from porous GaN formed by EC etching is demonstrated. This idea can be further extended to release InGaN/GaN MQW LED structures overgrown on a porous-GaN template formed by EC etching [62]. PEC- or EC-based transfer techniques have some advantages, compared with other ELO methods. Since the release layer is a GaN-based material (e.g., InGaN), the epi-layer quality can be maintained, and only one metal-organic chemical vapor deposition (MOCVD) growth cycle is

needed, without introducing an extra dissimilar release layer which is commonly deposited by different equipment. One potential disadvantage, however, is the high surface roughness after lift-off. Furthermore, large-scale lift-off based on these techniques remains challenging.

3. Layer Transfer by Laser Lift-Off (LLO)

While ELO discussed in the previous section has achieved good success in some particular cases, the nature of wet etching also tends to cause partial damage to the semiconductor layer to be released. Finding a chemical etchant which is absolutely inert to the semiconductor layer but has a very high etch rate for the sacrificial layer is very difficult. The long etch duration for the wafer-level of ELO in many cases is also another constraint for fast production. Furthermore, wet etching is commonly not environmentally friendly, and is also hazardous in many cases. For these reasons, a few “dry” lift-off mechanisms are explored for layer transfer to minimize wet etching-induced damage and accelerate the lift-off.

One example of dry lift-off for layer release is LLO [70][71][72][73][74][75][76][77]. As schematically shown in Figure 1b, LLO makes use of the difference in absorption of the laser light between the substrate and the layer being released. In the case of GaN LEDs grown on a sapphire substrate, for example, the GaN epi-layer has a band gap of about 3.3 eV, whereas the sapphire band gap energy is ~ 9.9 eV. Short-wavelength laser light is therefore transparent for the sapphire, and but strongly absorbed in the GaN layer, thereby generating intense heat. This localized heat leads to the decomposition of the GaN near to the GaN/sapphire interface into Ga droplets and nitrogen gas, thereby separating the epi-layer from the substrate.

One particular application of this technique is the wafer-scale layer transfer of a GaN thin film to a support substrate. To assist the laser lift-off, the wafer is commonly fixed onto a temporary substrate by wafer bonding or adhesive bonding. One example [71] of such a strategy is demonstrated by Wang et al. (Figure 6). GaN wafer grown on sapphire was bonded with a Mo substrate using Ni/Au as the bonding layer. LLO was conducted to take off the sapphire substrate. A further bonding and subsequent annealing were applied to the released GaN layer on the Mo substrate. As a result, the resulting two-inch-diameter GaN template showed improved stability and a minimized stress state. Similarly, successful thin-layer transfer of 2-inch GaN via LLO has also been achieved by other support substrates including GaAs and polydimethylsiloxane (PDMS) [73].

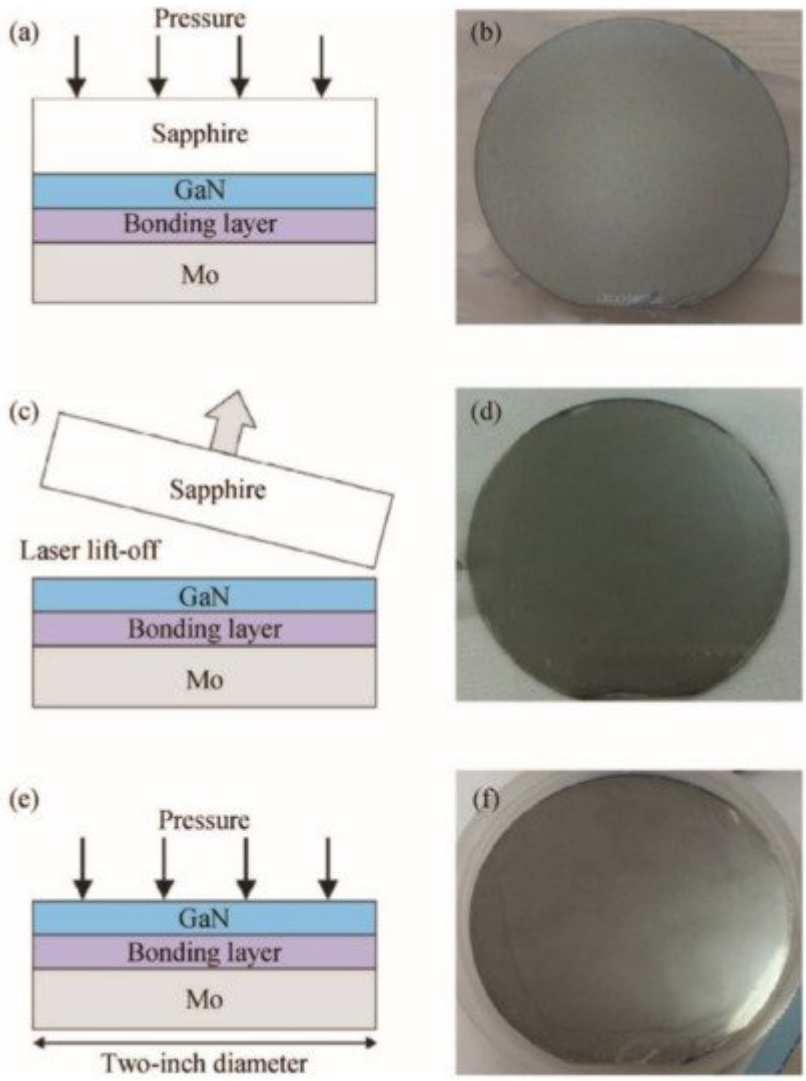

Figure 6. Schematic diagram of sample (**a**) after first bonding, (**c**) after laser-lift-off, and (**e**) after second bonding; image of the 2-inch-diameter sample after it went through (**b**) first bonding, (**d**) laser-lift-off, and (**f**) second bonding. Adapted with permission from [71]. Copyright IOP Science, 2016.

Many investigations indicate that LLO can also be used for fabricating free-standing GaN substrates with large thickness [70][73][75][76]. The free-standing GaN wafer size by LLO was limited to 1.5~2 inches in earlier investigations [75][76], but 4-inch free-standing GaN wafers have been demonstrated recently [70]. Major factors preventing the achievement of large, thick GaN templates include cracks induced by the thermal strain relaxation and laser-induced shock waves, causing damage at the N-polar face of GaN. It was reported that a heating plate above 800 degrees is helpful to release the compressive strain and avoid cracks during LLO. Laser spot size is another critical parameter affecting the laser-induced damage [70].

The laser lift-off technique is also applicable for fabricating flexible devices [78][72][74][79][80][81]. An example of the process flow for making flexible OLED displays based on LLO is shown in Figure 7. A sacrificial layer of polyimide [74] or α-GaOx [79] is formed on glass substrate. OLED devices are then formed on the sacrificial layer. Laser beam scanning results in intense heat generated in the interface between the sacrificial layer and glass substrate.

Consequently, the sacrificial layer is ablated, resulting in the top OLEDs becoming delaminated from the substrate. This technique is now applied in large-volume production of flexible OLED display screens [74].

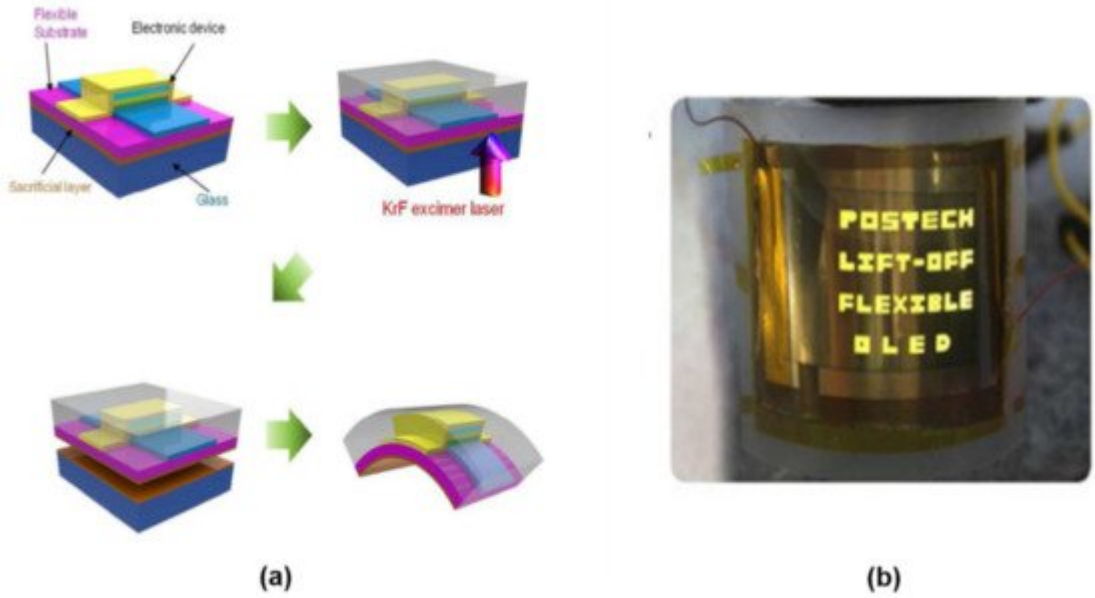

Figure 7. (**a**) Schematic diagram of the process flow for fabricating flexible OLED display by LLO. (**b**) The corresponding flexible OLED display fabricated by laser lift-off (LLO) based on the technology shown in (**a**). A 248 nm excimer KrF laser with a pulse width of 25 ns is used for the LLO. Adapted with permissions from [79]. Copyright Royal Society of Chemistry, 2014.

The LLO method is fast and scalable for any wafer size. For example, a 2” wafer, in principle, could be lifted off in a few seconds. However, in order to achieve high-quality transferred layers free from damage by laser lift-off, the beam quality and control must be well controlled. The cost of LLO facilities is another disadvantage that restricts its availability to regular users.

4. Layer Transfer by Mechanical Release

Mechanical release relies on mechanical force to separate the semiconductor layer from a growth substrate and transfer it to a support substrate. Broadly speaking, there are three major mechanical release approaches: spalling, 2D layer assisted peeling, and water-induced de-lamination.

4.1. Stress-Induced Delamination

Stress-induced delamination, or spalling [82][83][84][85][86][87][88][89][90][91][92], refers to a phenomenon where a layer with tensile stress tends to peel away from the substrate where the layer is grown, accompanied by the removal of a portion of the substrate material (Figure 8a). The mechanism behind spalling (or cracking) is due to the edge load created by the tensile stressor which guides the crack to be propagated at an equilibrium depth below the interface [83][85].

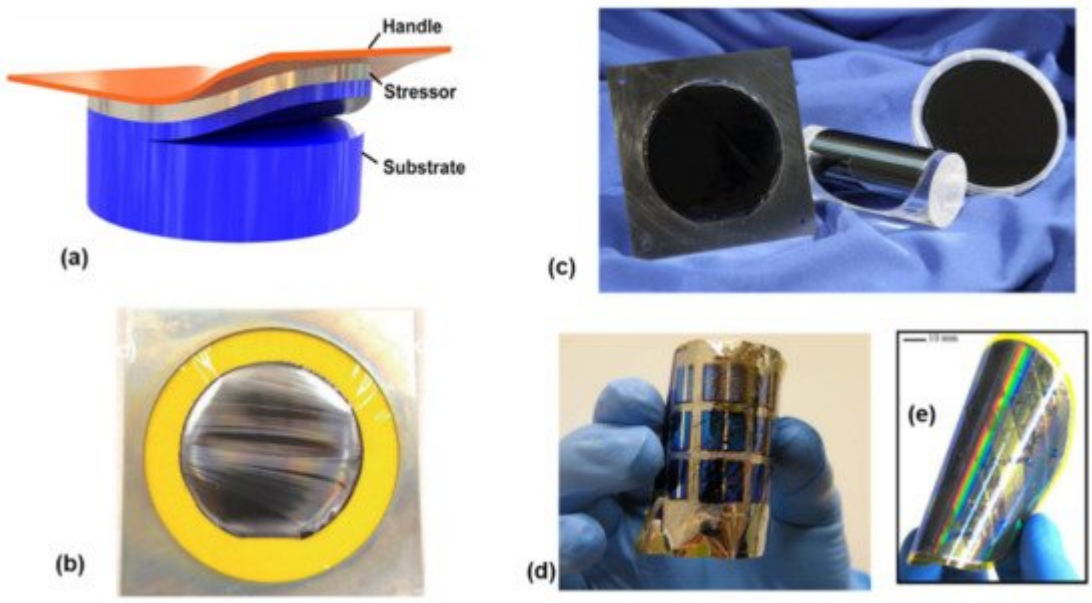

Figure 8. (**a**) Sketch of the mechanical spalling. Adapted from [86]. (**b**) Optical image of the released GaN film. Adapted with permission from [85]. Copyright IOP Science, 2013. (**c**) Optical images of Si on plastic mounted in a handling frame, 8 µm thick III–V multijunction layers on tape and mounted on a cylinder, and the bulk Si substrate from which the 20 µm thick layer was removed (from left to right). (**d**) Solar cells. Adapted with permission from [83]. Copyright IEEE, 2016. (**e**) flexible CMOS circuits fabricated by spalling techniques. Adapted with permission from [88]. Copyright American Chemical Society, 2012.

To achieve a controllable fracture and continuous film transfer, a tensile stressor layer with suitable thickness is coated on the substrate, followed by attaching a tape as the handle layer. A small force is then applied on the handle layer, resulting in forming a crack at a predetermined depth in the substrate. By mechanically guiding the handle layer, this crack can be guided and propagated in a controllable manner, resulting in transferring a portion of the material from the substrate to the handle layer [86].

This effect has been known for many years, and now it is possible to make use of this effect to achieve wafer-scale layer transfer of a variety of materials and devices, as shown in Figure 8. For example, silicon [82][87], InGaP/(In)GaAs [89], and GaN [85][91] have been successfully released by spalling. A wide range of flexible devices have also been demonstrated by spalling, including solar cells [83][84][89], LEDs [85][91], CMOS [86][88][92], etc. The figure below shows, for example, representative images of the full-wafer scale semiconductor layers and devices transferred by using this technique (Figure 8b–e).

Compared with epitaxial lift-off, stress-controlled spalling is much simpler, independent of area, and does not require the use of specialized etch layers. Substrate reuse is also demonstrated, opening up the prospect of cost reduction. One disadvantage of this technique, however, is fracture depth (or the thickness of the transferred layer) control, which is largely dependent on a variety of factors such as the stress amplitude, stress layer thickness, the stress layer material, and also the substrate material [86]. Accurate control of the thickness of the transferred layer induced by the spalling is therefore possible but extremely challenging. Another challenge lies in the residual stress

and slight curvature that the layers possess after spalling. To process such thin, stressed films requires the development of particular film handling strategies and equipment. The third challenge lies in the high roughness of the released layer. For instance, roughnesses up to 500 nm root mean square (RMS) have been reported for released GaN [91]. The high roughness of the released layer is undesirable for subsequent device fabrication and integration.

4.2. 2D Layer-Assisted Delamination

2D layer-assisted delamination exploits the weak adhesion of the thin layer grown on layered 2D semiconductors [93][94][95][96][97][98][99][100][101][102][103][104][105][106][107][108][109][110]. This technique is also referred to as van der Waals (VDW) epitaxy [110] (Figure 9). Applying a mechanical force will break up the weak adhesion, and induce the delamination of the thin film from the 2D layered semiconductor. This method can potentially be used to obtain wafer-scale layer transfer at a low cost. Thanks to the advancement in epitaxial growth, VDW growth of high-quality III-nitride on such 2D semiconductor layers has been demonstrated, despite the large lattice mismatch. Various 2D layered materials, such as boron nitride [97][98][101][103] and graphene [93][94][95][96][99][100][102][104][105][106][107][108][109], have been explored to assist the lift-off of the thin semiconductor layers grown on 2D layered materials.

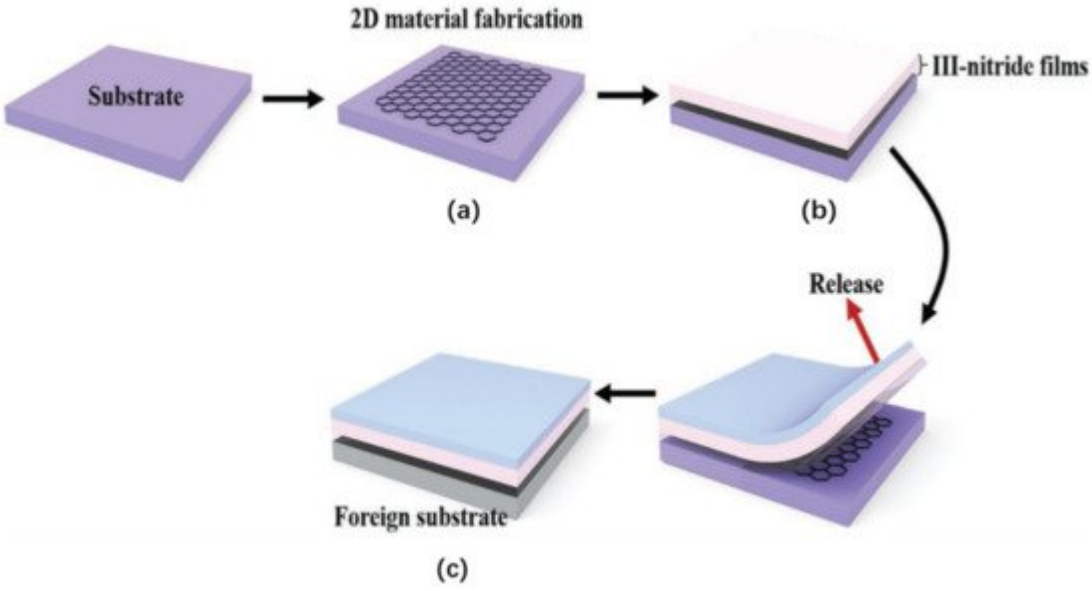

Figure 9. Schematic of 2D layer-assisted layer transfer, including three steps: (**a**) 2D material fabrication, (**b**) VDW epitaxy of III-nitride film, and (**c**) transfer printing onto foreign substrate. Adapted with permission from [110]. Copyright John Wiley and Sons, 2019.

Kobayashi et al. demonstrated the high quality of growth AlGaN/GaN LED layers on a boron nitride single-crystal layer [97]. The boron nitride layer has two functions. Besides the role for subsequent lift-off, it also acts as the buffer layer for nucleation of the high-quality AlGaN/GaN LED layer. To prevent from formation of polycrystalline GaN, an AlGaN layer is first deposited on the BN layer, followed by growing the final GaN LED layer structures. Due to its weak adhesion on the boron nitride, the LED layer can then be readily separated from the substrate to an indium sheet by weak peeling. Based on similar techniques, prototype vertical LEDs have also been demonstrated by the

same group [98]. However, only centimeter-scale layer transfer has been demonstrated. Wafer-scale transfer based on BN needs to be explored. To overcome the size limit, one possible route is to grow a BN monolayer on a modified substrate with a quasi-3D mainspring shape in a furnace tube, instead of the conventional flat substrate [103]. This allows a high-quality h-BN monolayer with a size up to 25 inch to be grown, which can be then transferred to sapphire substrate for growing GaN. A 2-inch GaN wafer free of misfit strain grown on a BN monolayer has been achieved based on this technique.

Graphene-assisted growth has also been explored for fabricating free-standing semiconductor membranes [93][100][102][104]. Since the nucleation of atoms on a pristine graphene surface is remarkably suppressed due to the inert surface reactivity of graphene, earlier studies were therefore mainly focused on growing 3D microstructures on graphene. For instance, Chung et al. demonstrated the growth of regular GaN microdisk arrays on graphene dot patterns using epitaxial lateral overgrowth (ELOG) [102]. In another example, GaN microrods on graphene were demonstrated [100].

The 2D nucleation difficulty, however, can be overcome by introducing an intermediate layer. For instance, Chung et al. [94] demonstrated that ZnO nanowalls grown on graphene can assist the subsequent growth of 2D GaN LED layers (Figure 10). Due to the same crystal structure and small lattice mismatch with GaN, epitaxial GaN films are formed on the nanowalls in a manner similar to the lateral overgrowth, and eventually a flat GaN overgrowth layer can be formed. Such high-quality GaN LED layers grown on graphene allow the fabrication of LEDs transferred to various substrates, including glass, metal, and plastic, by simple mechanical peeling, and strong blue emissions have been obtained from such devices.

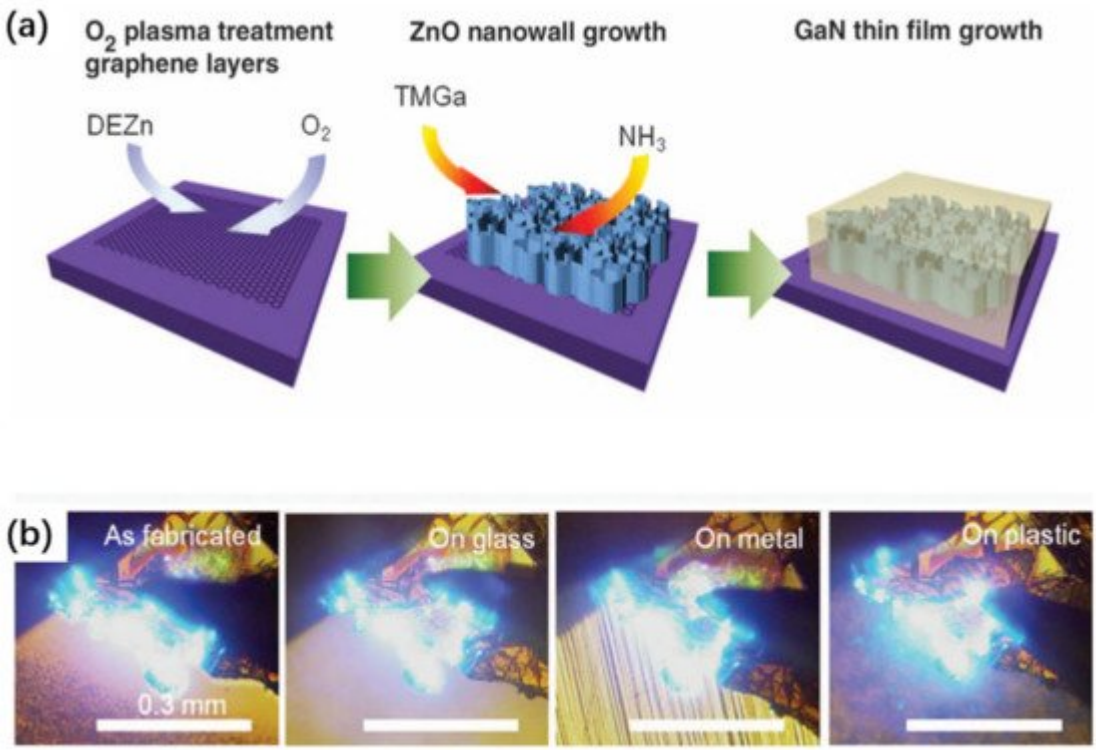

Figure 10. (**a**) Schematic illustrations of fabrication processes for epitaxial GaN thin films. (**b**) Optical images of light emissions from the as-fabricated LED on the original substrate and transferred LEDs on the foreign metal, glass, and plastic substrates. Adapted with permission from [94]. Copyright The American Association for the Advancement of Science, 2010.

In another study, to overcome the nucleation difficulty in 2D growth on graphene, an AlN buffer layer was introduced between the growth layer and graphene [105]. The graphene layer was grown on sapphire substrates by a catalyst-free atmospheric pressure chemical vapor deposition (APCVD) process, instead of using the complex transfer process of ex situ-grown graphene. An AlN buffer layer is then deposited on the nitrogen plasma-treated graphene to promote the GaN nucleation. The epitaxy is then finalized by growing GaN LED layers on the AlN/graphene buffer [105]. The APCVD method allows the high-quality growth of 2-inch single-crystal graphene. Due to the strain relaxation by the graphene, the as-prepared GaN shows significant improvements in the epitaxial quality, with a dislocation density as low as $1.7 \times 10^7 cm^{-2}$. The fabricated LED devices therefore are able to deliver much high optical power output than the device directly grown on sapphire.

Instead of using intermediate buffer layers, the nucleation difficulty can also be addressed by using a different growth strategy based on an off-angle substrate [93]. Such an off-angle substrate can remarkably promote the atom nucleation at the periodically distributed step edges, resulting in forming high-quality 2D materials grown directly on graphene. A good example based on this strategy is shown in the paper [93] (Figure 11). Miscut SiC substrates are used to grown graphene. Then, single-crystalline GaN films on graphene/SiC substrates are grown by using periodically distributed steps as the GaN nucleation sites. The following step is to deposit a stressor metal (Ni) and attach a thermal release tape to separate entire GaN films from the graphene surface and transfer the released GaN to host substrates. Fully functional blue light-emitting diodes (LEDs) have been demonstrated by this technique. SiC substrate reuse is also demonstrated.

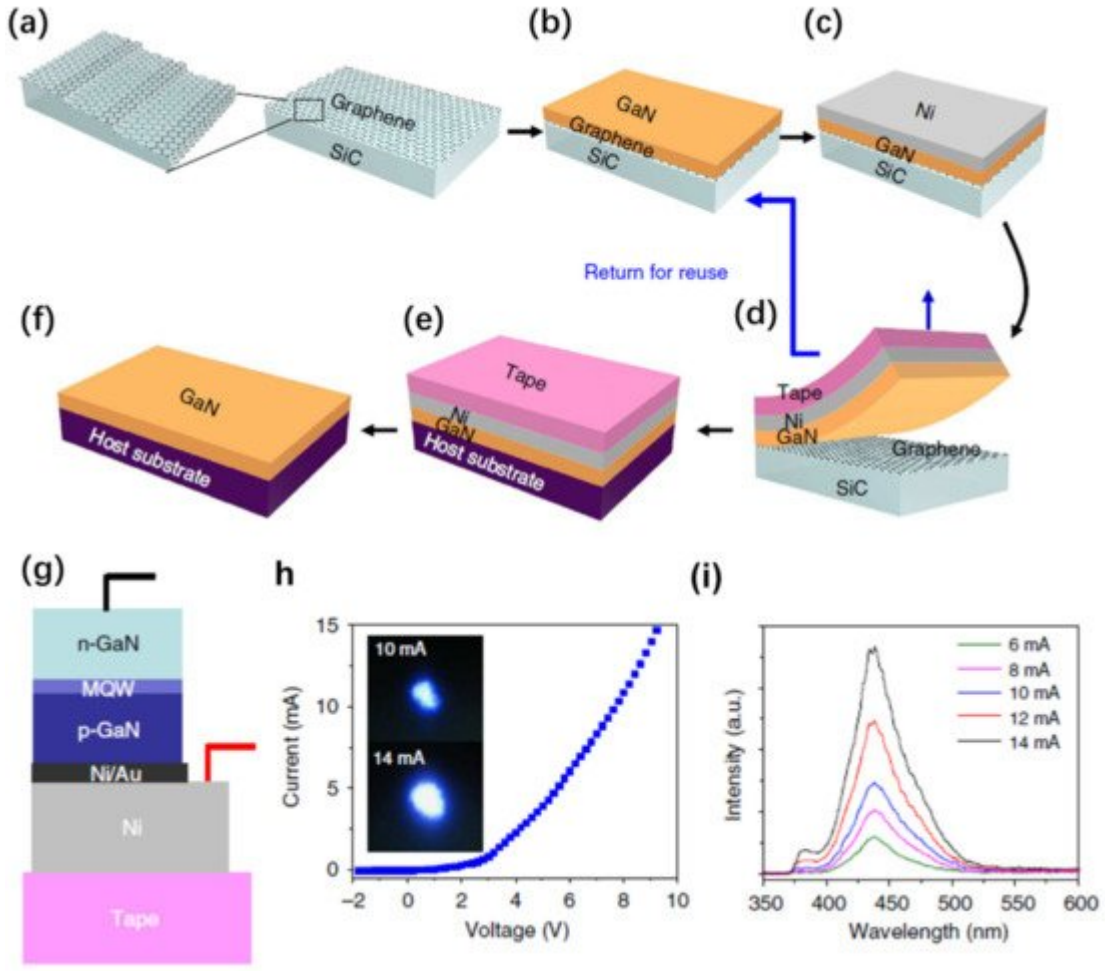

Figure 11. Schematic of a method for growing/transferring single-crystalline thin films on/from epitaxial graphene (**a**–**f**). (**g**) Schematic of a transferred visible LED device on the tape. (**h**) I–V characteristic of a transferred LED stack measured by applying positive bias on Ni and negative bias on n-GaN. The pictures of the LED emitting blue light are displayed in an inset. (**i**) Electroluminescence (EL) spectra of a transferred LED stack taken as a function of injection current. Adapted from [93].

Compared to the thermal, chemical, and mechanical approaches, the abovementioned strategy is a simple and feasible transfer technique with no need for additional procedures or equipment. This technique is similar to spalling, but one distinct merit is the accurate thickness control of the released layer—the thickness of the layer to be released is controlled by epitaxial growth, rather by the fracture depth decided by the stress amplitude. The other advantage is the reduced stress required for transfer, compared with spalling. Finally, the separation interface is smoother due to the 2D buffer layer not allowing covalent bonds between the epi-layer and the substrate.

4.3. Water-Assisted Delamination

Water-assisted delamination exploits the phenomenon of water-assisted debonding at the interface between a metallic layer (e.g., Ni) and an oxide layer (SiO2) [111][112][113]. This debonding in turn lifts off the upper layer from the original SiO2/Si substrate. The underlying mechanism is due to the water-induced decrease in the critical adhesion energy of the metal–SiO2 interface, which can be over 70% [112].

The discovery of this technique can be credited to Lee and coworkers [111][112]. An example [111] of an application using this technique is the transfer of thin-film solar cells (TFSCs) onto arbitrary substrates (Figure 12). TFSC films are deposited on Ni-coated SiO2/Si substrates, followed by standard microfabrication to form TFSC devices. A tape is attached to the TFSC surface as the temporary holder. The entire sample is then loaded into a water bath. A small peeling force is then applied at the tape edge to promote water penetration into the interface, and thus inducing the delamination of the TFSC devices from the substrate. The final step is transferring the released TFSC devices to the receiver substrates by sticking and removing the tape. Based on this technique, high-efficiency solar cells transferred to arbitrary substrates, such as cell phones, business cards, and glass windows, have been demonstrated. Such transferred devices maintained the same efficiency of 7.5%, implying no obvious degradation caused by the transfer process.

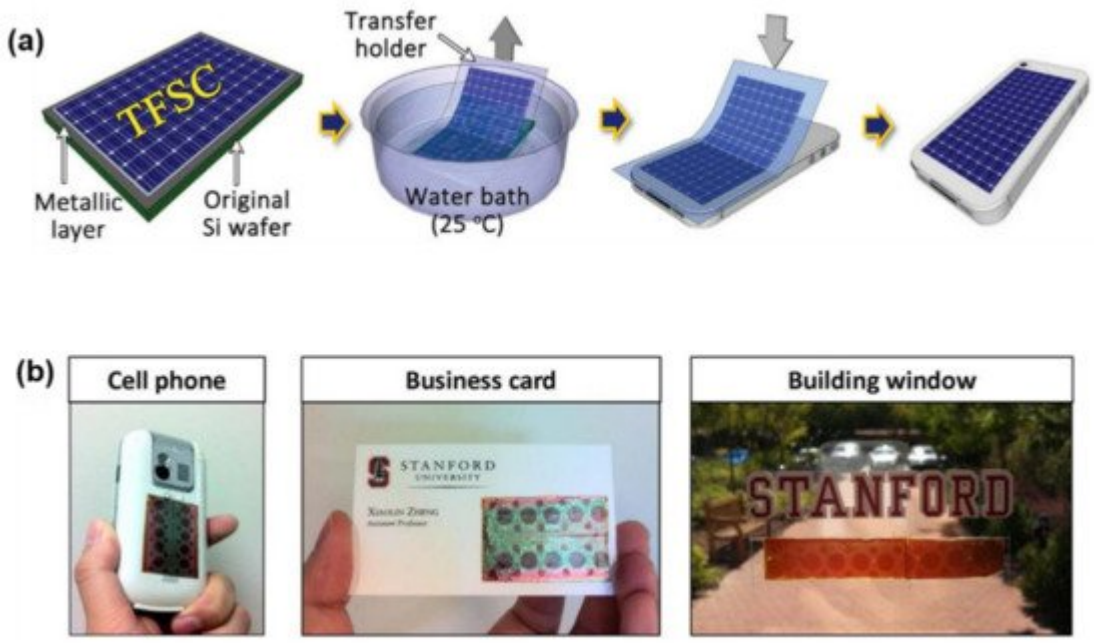

Figure 12. (**a**) Procedures of the peel-and-stick process. (**b**) Solar cells on cell phone (left), business card (middle), and building window (right). Adapted from [111].

In a more recent work [113], the same method is exploited to fabricate a wide range of thin-film nanoelectronic devices, such as a transferred Ag nanowirebased resistor, Si nanoribbon-based p-i-n diode, Si nanomembrane-based transistor, Si nanomembrane-based thin-film capacitors, nanomembrane-based MOSFETs, and a hybrid photodiode system that combines p-doped Si NM and n-doped MoS2 (Figure 13). The process has two primary steps: (i) transfer printing various single-crystalline semiconducting nanomaterials onto specific locations of a SiO2/Si wafer in a single device layout, followed by conventional CMOS fabrication to form electronic circuits on the wafer, and (ii) physically separating the entire layer of the completed thin-film nanoelectronics from the fabrication SiO2/Si wafer, which can be then pasted onto an arbitrary kind of supporting substrate or surface. The technique discussed here is wafer-recyclable, environmentally friendly, and cost-effective, showing good prospects for wafer-level production and integration of thin-film devices onto a single substrate.

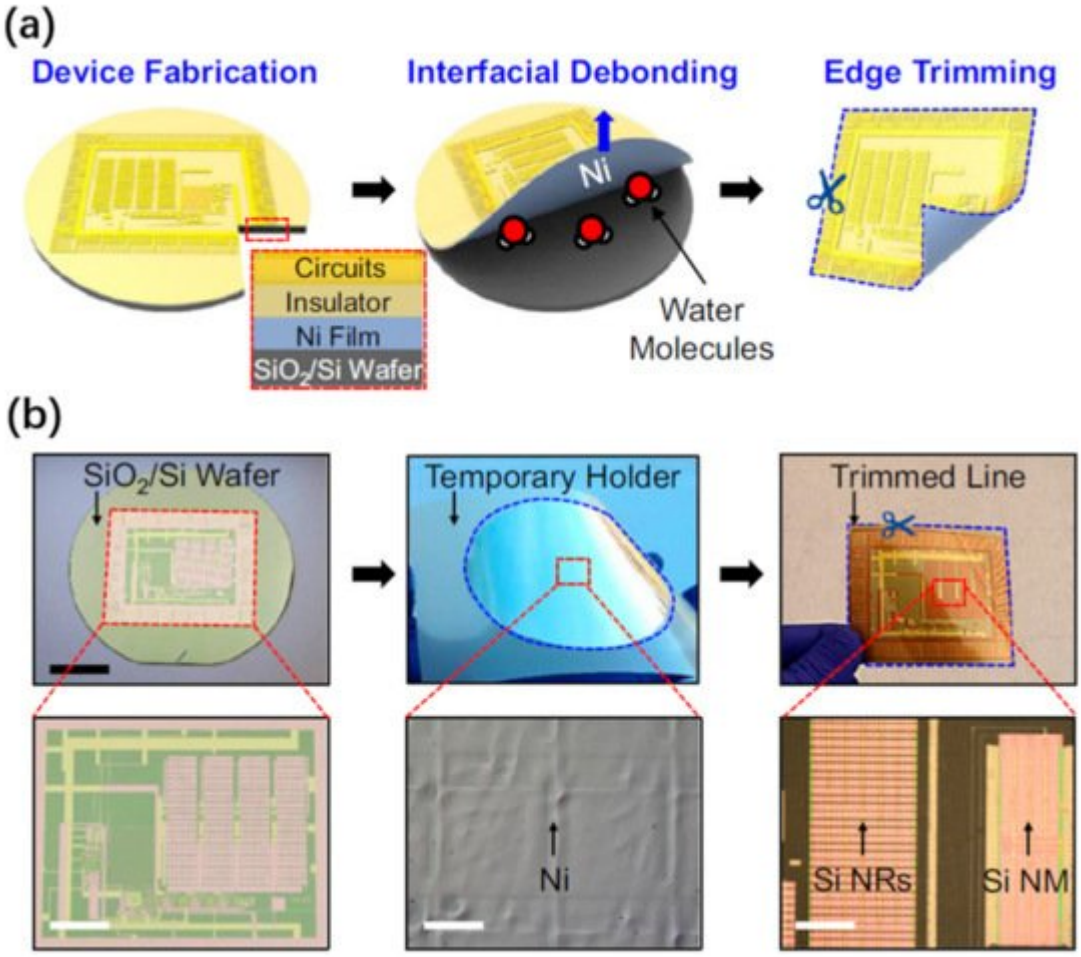

Figure 13. (**a**) Schematic illustrations of key steps for physically liberating thin-film nanoelectronics from a fabrication SiO2/Si wafer in water. (**b**) Optical images of the thin-film nanoelectronics on the SiO2/Si wafer (left), and peeled with a thermally releasable tape (middle), and then trimmed neatly (right). The bottom frame shows the corresponding microscope images. Si NRs in (**b**) stands for Si nanoribbons, and Si NM in (**b**) refers to Si nanomembrane. Adapted from [113].

5. Layer Transfer by Smart Cut

Smart Cut, or ion cut, is a technique of exploiting both ion implantation and wafer bonding to transfer ultrathin single-crystal layers from a donor substrate to a receiving substrate. This technology has been commercialized for the fabrication of silicon-on-insulator (SOI) wafers for many years [4], but it has also been explored for fabricating free-standing GaN membranes recently [114][115][116][117][118][119][120][121]. Taking splitting GaN, for example, the key processing steps of ion cut [114] are schematically shown in Figure 14a. A free-standing GaN template is prepared by depositing a thick GaN layer on a sapphire substrate, followed by LLO. The N-face of free-standing GaN is then implanted with H^+ ions after lapping and chemical mechanical polishing. Argon atom beam irradiation on the N-face GaN and sapphire surfaces under vacuum is then conducted, in order to form chemically active dangling bonds. The next step is bonding the free-standing GaN to another sapphire substrate via plasma-treated hydrophilic bonding. Afterwards, the layer transfer is carried out in a furnace by annealing GaN/sapphire. Finally, the

implantation-induced damaged layer on the low temperature grown GaN (LT-GaN) surface is removed using a dry etcher, resulting in LT-GaN transferred to the receiving wafer. Based on this technique, both a free-standing GaN template and GaN layer transferred to the receiving substrate with a wafer size up to 4 inches were demonstrated, as shown in Figure 14b,c.

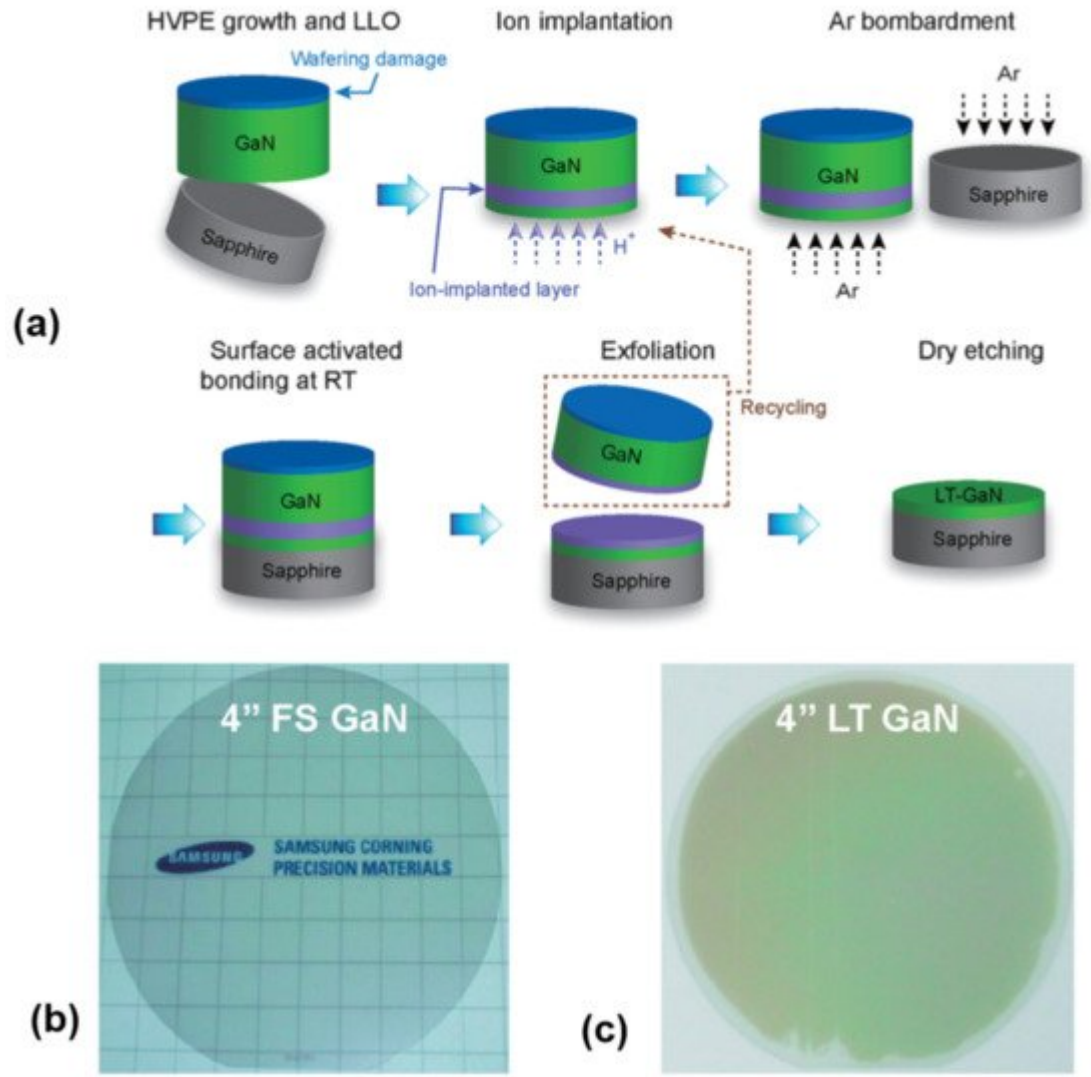

Figure 14. (**a**) Schematic illustrations of key steps for ion cutting techniques for GaN layer transfer. (**b**) Four-inch free-standing GaN template, and (**c**) transferred 4-inch GaN layer on the sapphire substrate. Adapted with permission from [114]. Copyright IOP Science, 2013.

One of the distinguishing features of the ion cut process is the production of multiple templates from a single donor wafer, thereby reducing the cost per template without compromising the crystalline quality. Another advantage is that the layer thickness can be finely controlled with nanometer-scale accuracy. For instance, with Smart Cut techniques, wafer-scale processed silicon films in the range of 0.2 to 1 μm in thickness have been reported.

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